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The University of Sheffield
Electrical and Electronic Engineering

Systems Design Analysis – Component Tolerance Assignment

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1 Contents

2 Introduction

This report outlines the results of a set of Systems Design exercises surrounding the effect of Component Tolerance on the operation of electronic circuits. Three circuits will be analysed; a Potential Divider, Low Pass Filter and Voltage Limiting circuit.

Extreme Value and Monte Carlo Analysis will be used to produce graphs of the effect of Component Tolerance on the key operating characteristics of each of these circuits, these results will be compared to sample specification for the circuits performance. This will allow analysis of values such as expected manufacturing yield and circuit loading.

Ultimately this report aims to show how Systems Design Analysis and Modelling can be used to increase the reliability and repeatability of the manufacture and operation of a circuit by calculating the tolerance values its constituent elements must adhere too.

3 Potential Divider Circuit

This section outlines the Systems Design Analysis performed on the Potential Divider Circuit shown in **Figure 3.1**. Extreme Value and Monte Carlo Analysis will be performed on the circuit to show the effect of Resistor Tolerance on the Voltage Division Ratio. This analysis will then be used to produce information on circuit Yield with respect to Resistor Tolerance.

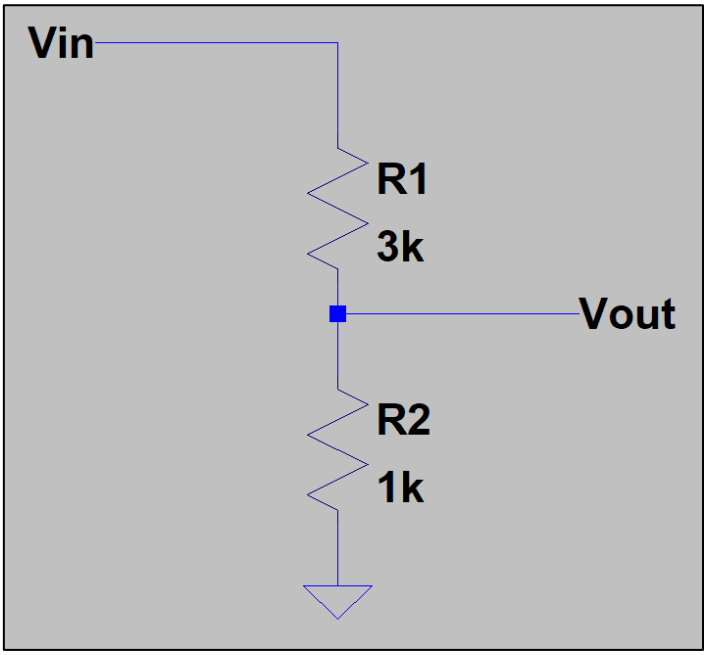

Figure 3.1: Potential Divider Circuit [3]

3.1 Extreme Value Analysis

Extreme Value Analysis was used to form an expression for the Tolerance in Voltage Division Ratio (ΔG) with respect to the Resistor Tolerance ΔR, where G is calculated as shown in **Equation 1**. ΔG was calculated by subbing **Equation 2** and **Equation 3** into **Equation 4** along with the specification values from **Table 3.1**. Simplification of this equation lead to **Equation 5**. All calculations were performed with the assumption that ΔR1 = ΔR2 = ΔR.

$$G = \frac{Vout}{Vin} \tag{1}$$

$$G_{max} = \frac{R2(1+\Delta R)}{R1(1-\Delta R)+R2(1+\Delta R)} \quad (2)$$

$$G_{min} = \frac{R2(1-\Delta R)}{R1(1+\Delta R)+R2(1-\Delta R)} \quad (3)$$

$$\Delta G = \frac{G_{max}-G_{min}}{2\times Gnom}\times 100 \quad (4)$$

$$\Delta G(\pm\%) = \frac{6\Delta R}{4-(\Delta R)^2}\times 100 \quad (5)$$

Potential Divider Circuit - Specification	
R1	3kΩ
R2	2kΩ
Nominal Voltage Division Ratio (Gnom)	0.25
Voltage Division Ratio Tolerance	±2%

Table 3.1: Potential Divider Circuit Specification [2]

Equation 5 gives the Voltage Division Ratio Tolerance as a percentage of the Nominal Voltage Division Ratio shown in **Table 3.1**. **Equation 5** was then used with a range of Resistor Tolerance values to generate the Voltage Division Ratio Tolerance values shown in **Table 3.2**.

Potential Divider - Voltage Division Ratio Tolerance		
Resistor Tolerance (+/-%)	**Voltage Division Ratio Tolerance (+/-%)**	**Meets Specification of (+/-2%)?**
1	1.5	Yes
2	3.0003	No
5	7.5047	No
10	15.0376	No

Table 3.2: Potential Divider Voltage Division Ratio Tolerance Extreme Value Analysis

Table 3.2 shows that for the specification of the potential divider defined in **Table 3.1** to be met a Resistor Tolerance of ±1% must be used. We can also observe that the Tolerance in Voltage Division Ratio increases exponentially with increasing Resistor Tolerance, this is caused by the 2nd Order Polynomial in the denominator of **Equation 5**.

3.2 Monte Carlo Analysis

To provide a more accurate model of the variation of Resistor Tolerance across a batch of Resistors Monte Carlo Analysis was used with the Uniform Distribution to produce Histograms of possible Voltage Division Ratios for 1%, 2%, 5% and 10% Resistor Tolerances. The Monte Carlo Analysis involved calculating the output Voltage of the Potential Divider (Vout) with 1000 sets of randomly generated Resistor Values. The data from these analyses can be seen in **Figure 3.2**, **Figure 3.3**, **Figure 3.4** and **Figure 3.5** respectively.

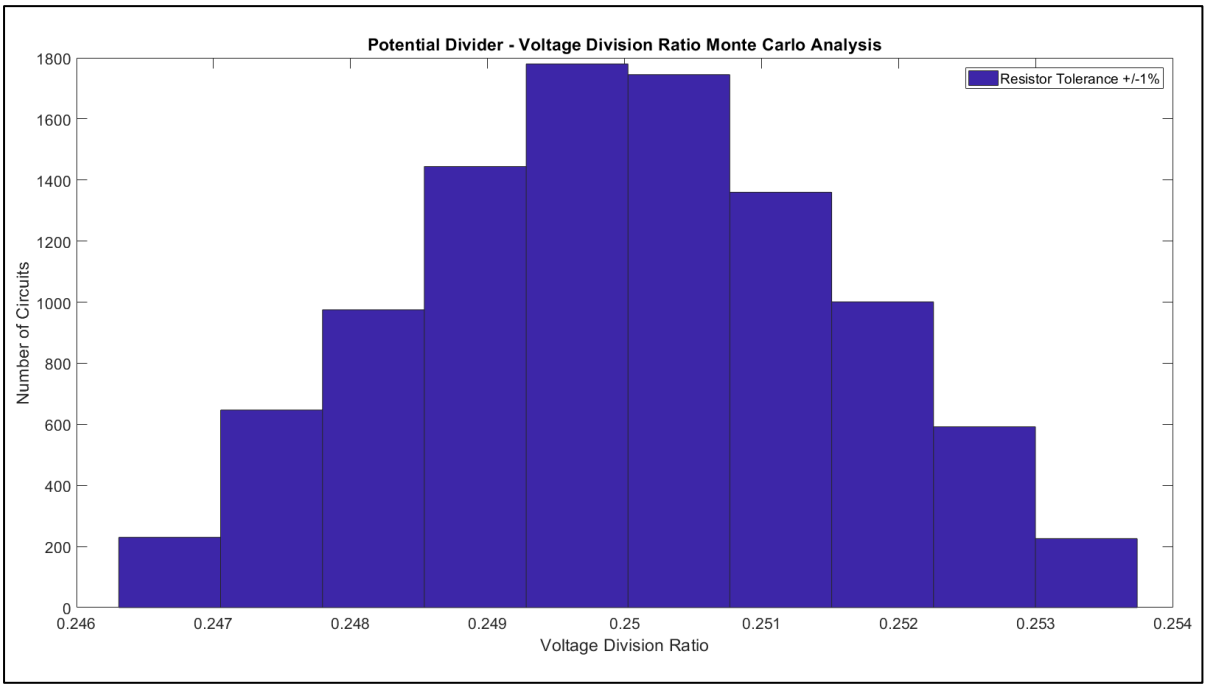

Figure 3.2: 1% Resistor Tolerance Monte Carlo Analysis - Voltage Division Ratio Histogram

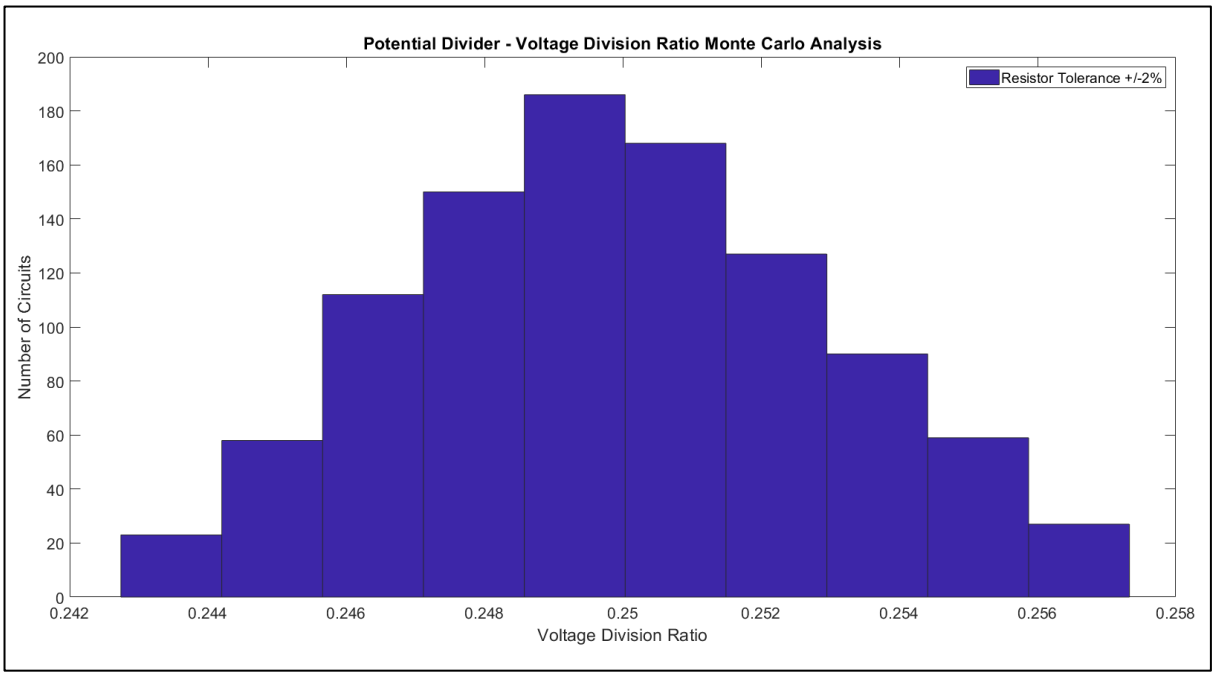

Figure 3.3: 2% Resistor Tolerance Monte Carlo Analysis - Voltage Division Ratio Histogram

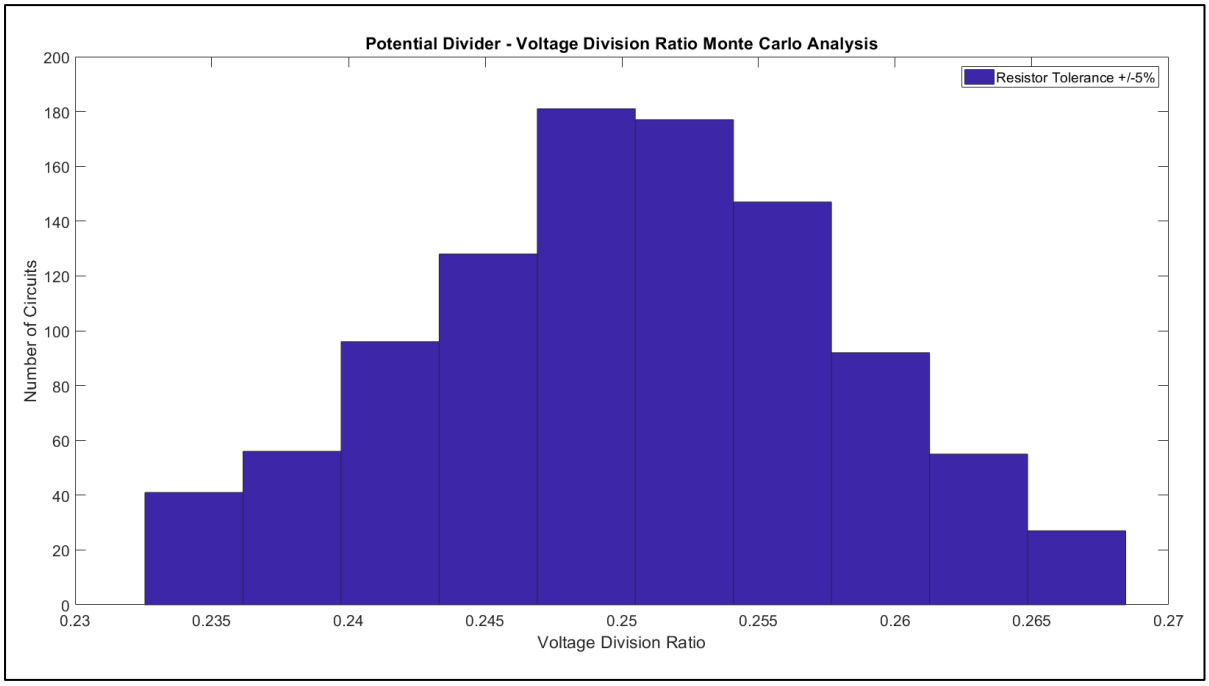

Figure 3.4: 5% Resistor Tolerance Monte Carlo Analysis - Voltage Division Ratio Histogram

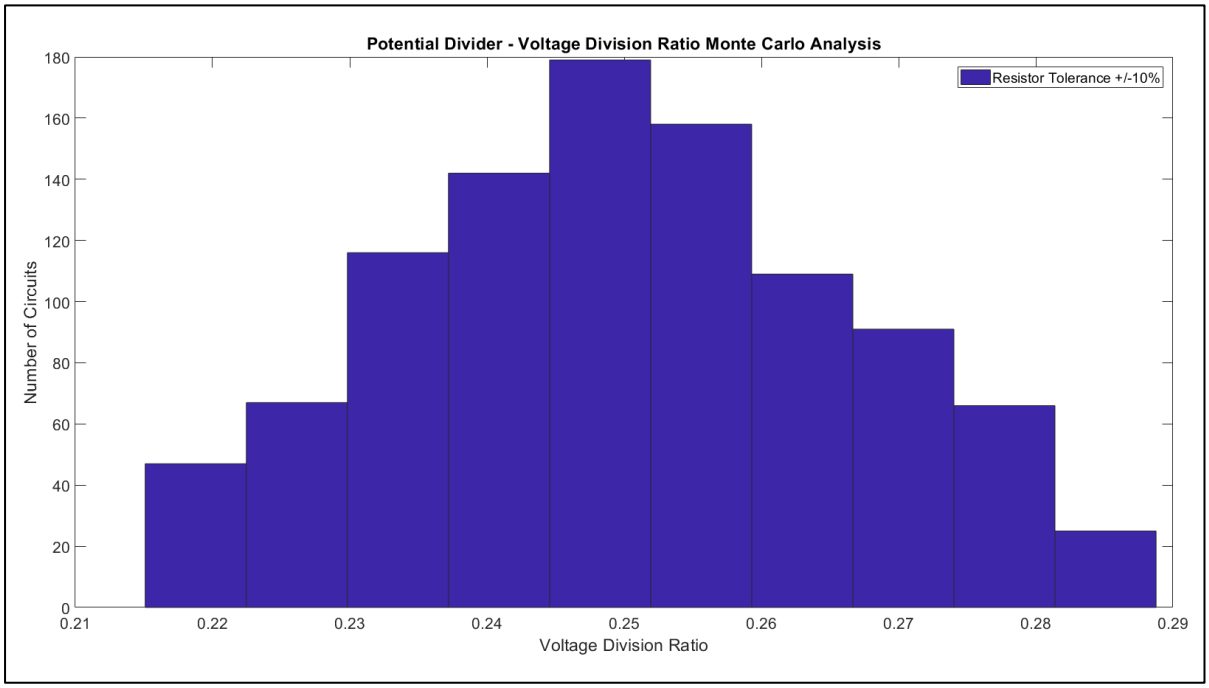

Figure 3.5: 10% Resistor Tolerance Monte Carlo Analysis - Voltage Division Ratio Histogram

Figures 3.2 to **3.5** show the same exponential increase in the extreme range of Voltage Division Ratio Tolerance as shown by the Extreme Value Analysis. However, they also show that when Resistor Tolerance is more accurately modelled by the Uniform Distribution the Voltage Division Ratio Tolerance will approximate to the Gaussian Distribution [1, p. 26]. This means that it is much more unlikely that the Voltage Division Ratio will be at the extreme of the acceptable tolerance, producing a higher manufacturing Yield even at higher Resistor Tolerances.

We can see why a Gaussian distribution is produced by looking at **Equations 2** and **3**; they show that for the extreme values of the Voltage Division Ratio to occur one Resistor must be at the extreme minimum possible value and one must be at the extreme maximum. The probability of this occurring is much lower than the probability of both resistor values being moderately far from nominal; thus, a bell-shaped curve of Voltage Division Ratio is formed.

A graph of Yield vs Resistor Tolerance can be seen in **Figure 3.6**; the Yield was calculated using **Equation 6**.

$$Yield = \frac{Number\ of\ Circuits\ within\ Specification}{Number\ of\ Circuits\ Produced} \tag{6}$$

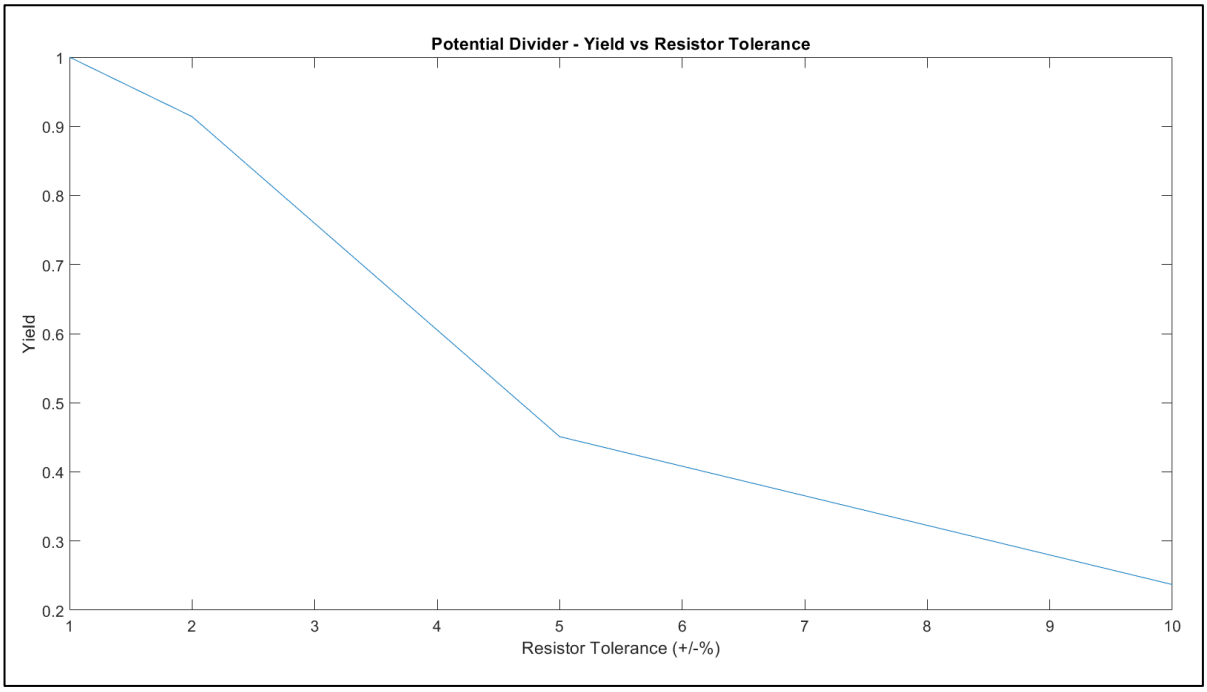

Figure 3.6: Potential Divider - Yield vs Resistor Tolerance for 1000 Circuits

Figure 3.6 shows that, as expected, the manufacturing Yield decreases with increasing Resistor Tolerance. We can observe that this decrease of Yield with Resistor Tolerance also follows an approximate exponential curve, this means that with increasing Resistor Tolerance the decrease in Yield falls exponentially. Thus, at high Resistor Tolerances very large increases in Yield can be achieved.

3.3 Maximum Theoretical Resistor Tolerance

Combining the techniques used in the previous two sub sections a theoretical maximum acceptable value of resistor tolerance can be calculated. This value was calculated by subbing the maximum acceptable Voltage Division Ratio Tolerance (±2%) into **Equation 5**, this resulted in a value of approximately ±1.33%.

This value was then verified using the same Monte Carlo Analysis technique used in **Section 3.2**. A graph of the output Histogram can be seen in **Figure 3.7**.

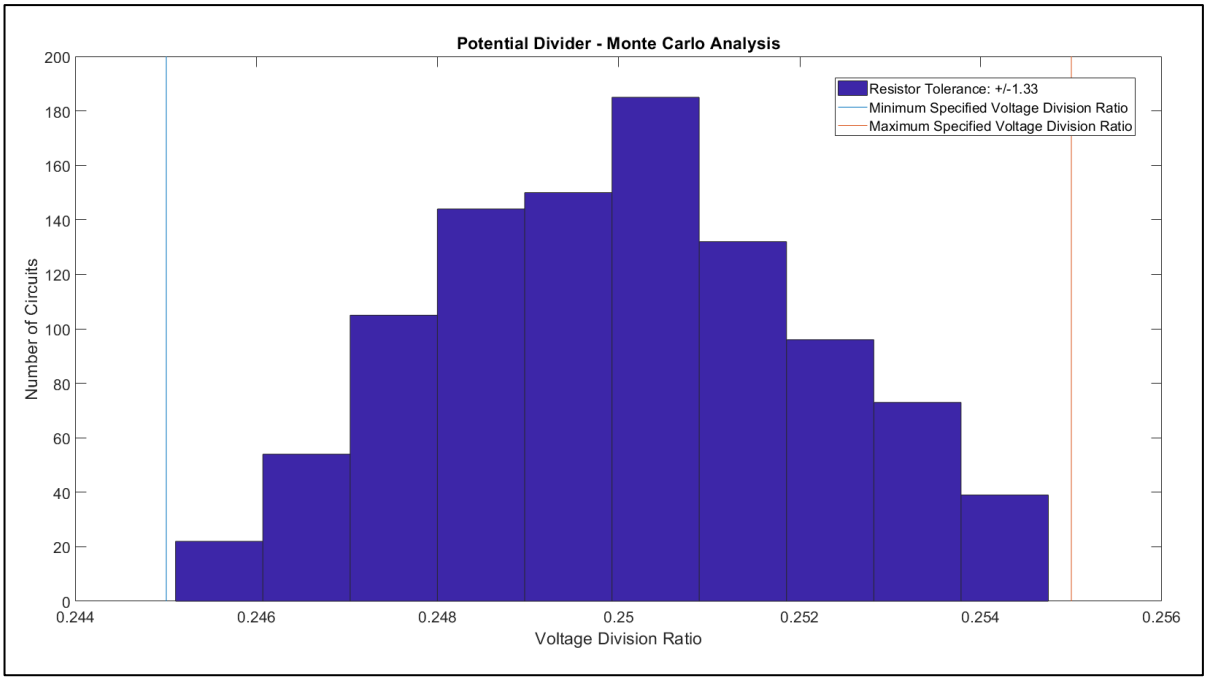

Figure 3.7: 1.33% Resistor Tolerance Monte Carlo Analysis - Voltage Division Ratio Histogram

Figure 3.7 shows that this value of Resistor Tolerance produces a Yield of 1. It also shows that the extreme Voltage Division Ratio values just fall within the specification from **Table 3.1,** confirming that this value of Resistor Tolerance is approximately the maximum that can be used whilst still achieving a Yield of 1 for this specification. This calculation is however, somewhat unhelpful, as you cannot easily purchase a Resistor Value with a tolerance of ±1.33%.

3.4 Conclusion

In this section we have shown that for the specification outlined in **Table 3.1** to be met the Tolerance of the Resistors used in the potential divider must be ±1% or lower, as calculated using Extreme Value Analysis and verified using Monte Carlo Analysis.

Theoretically a maximum value of approximately ±1.33% could be used for the Resistor Tolerance, however this is unrealistic as large quantities of Resistors with this tolerance are not available. As such ±1% is used as the first readily available tolerance that meets the specification.

We have also shown that Extreme Value Analysis is inaccurate when attempting to estimate a manufacturing Yield as Monte Carlo Analysis using a Uniform Distribution has shown that the Voltage Division Ratio follows a Gaussian Distribution. As such an acceptable Yield may be produced with a Resistor Tolerance higher than ±1% if the savings produced by purchasing lower quality resistors outweigh the costs of a lower Yield. This is however unlikely to be the case due to the gaps in widely available Resistor Tolerances.

Finally, we have shown that the graph of Yield vs Resistor Tolerance follows an exponential curve. This means that large increases in Yield can be produced by small decreases in Resistor Tolerance at the low end of the Tolerance value scale. This may well explain why the increase in price of switching from a 2% to a 1% Tolerance resistor is mostly greater than that of switching from a 10% to a 2% Tolerance Resistor.

4 Low Pass Filter Circuit

This section outlines the Systems Design Analysis performed on the Low Pass Filter Circuit shown in **Figure 4.1**. Extreme Value and Monte Carlo Analysis will be performed on the circuit to determine the effect Resistor and Capacitor tolerance have on the Corner Frequency (Δf_c). This results from this analysis will then be used to produce information on manufacturing Yield with respect to Resistor and Capacitor Tolerance.

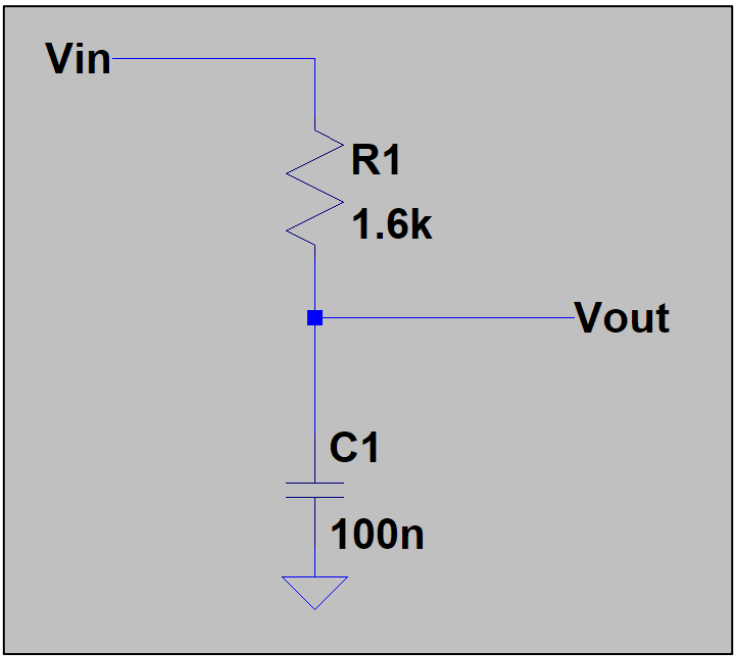

Figure 4.1: Low Pass Filter Circuit [2]

4.1 Extreme Value Analysis

As with the Potential Divider Circuit from **Section 3**, initially Extreme Value Analysis was performed to determine the range of Corner Frequencies the circuit would produce with varying Resistor Tolerances. Using the same method as used in **Section 3.1** an equation for the tolerance in the Corner Frequency was produced. **Equations 8** and **9** were subbed into **Equation 10** to produce **Equation 11**. The equation for the nominal Corner Frequency is given in **Equation 7**.

$$f_{c(nom)} = \frac{1}{2\pi RC} \tag{7}$$

$$\Delta f_{c(\max)} = \frac{1}{2\pi R(1-\Delta R)C(1-\Delta C)} \tag{8}$$

$$\Delta f_{c(\min)} = \frac{1}{2\pi R(1+\Delta R)C(1+\Delta C)} \tag{9}$$

$$\Delta f_c(\pm\%) = \frac{\Delta R + \Delta C}{2\pi f_{c(nom)} RC(1-\Delta R^2)(1-\Delta C^2)} \times 100 \tag{10}$$

Equation 10 gives the Tolerance in Corner Frequency as a percentage of the nominal Corner Frequency as calculated using **Equation 7**. **Equation 10** was in conjunction with the specification values from **Table 4.1** to produce the Extreme Value Analysis results shown in **Table 4.2**.

Low Pass Filter Circuit - Specification	
R	1.6kΩ
C	100nF
Nominal Corner Frequency	1kHz
Corner Frequency Tolerance	±5%

Table 4.1: Low Pass Filter Circuit Specification [2]

Low Pass Filter - Corner Frequency Tolerance			
Resistor Tolerance (+/-%)	Capacitor Tolerance (+/-%)	Corner Frequency Tolerance (+/-%)	Meets Specification of (+/-5%)?
1	10	11.0535	No
2	10	12.062	No
5	10	15.1093	No
10	10	20.2983	No

Table 4.2: Low Pass Filter Corner Frequency Tolerance - Extreme Value Analysis Results

Table 4.2 shows that for the Low Pass Filter Circuit specification defined in **Table 4.1** a Capacitor Tolerance lower than ±10% must be used. Currently all combinations of Resistor and Capacitor Tolerance shown in **Table 4.2** are more than ±5% of Corner Frequency Tolerance away from the specified Corner Frequency Tolerance. Given that the Resistor Tolerance is already low at ±1%, the Capacitor Tolerance must be lowered.

Again, as in **Section 3.1**, we can see that the Corner Frequency Tolerance increases exponentially with Resistor Tolerance. Again, this is due to the 2nd Order Polynomial on the denominator of **Equation 10**.

4.2 Monte Carlo Analysis

To provide a more accurate model of the variation of Resistor and Capacitor Tolerance across a batch of components Monte Carlo Analysis was performed on the Low Pass Filter Circuit. This analysis was completed by producing 1000 randomly generated Resistor and Capacitor values using the Gaussian Distribution. These randomly generated values were subbed into **Equation 7** to generate a Histogram of Corner Frequency. This analysis was performed with a Capacitor Tolerance of 10% in conjunction of Resistor Tolerances of 1%, 2%, 5% and 10%. The results from these analyses can be seen in **Figure 4.2**, **Figure 4.3**, **Figure 4.5** and **Figure 4.4**.

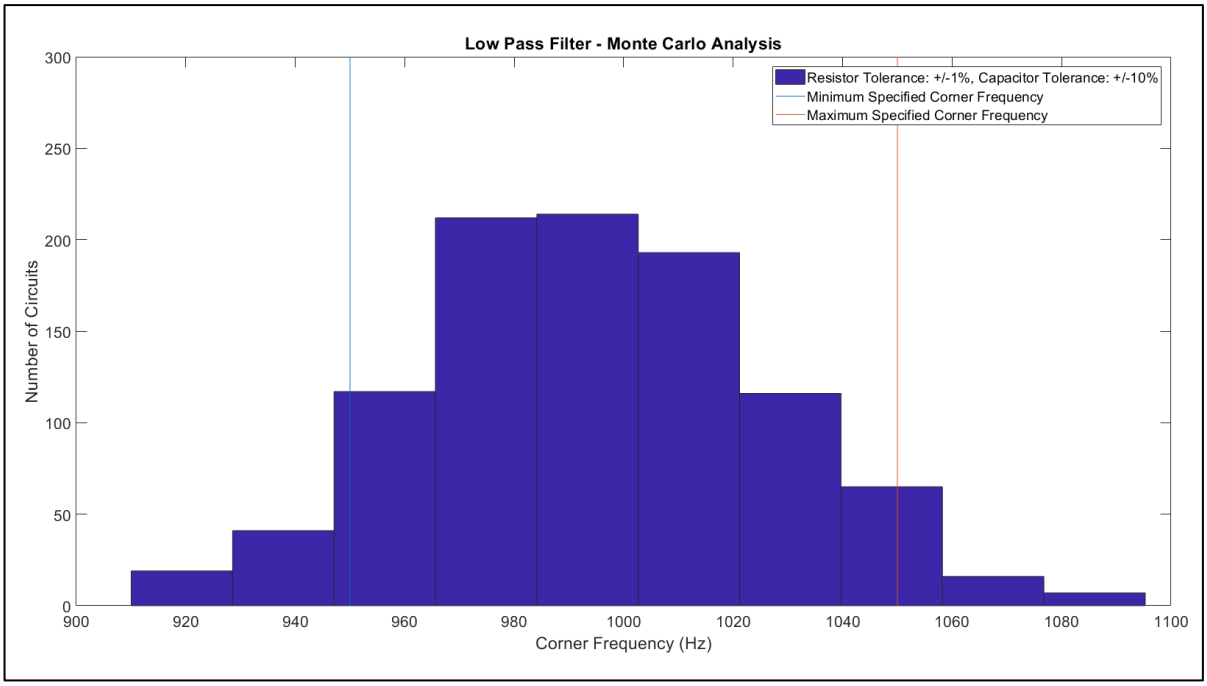

Figure 4.2: Corner Frequency Monte Carlo Analysis - 1% Resistor Tolerance

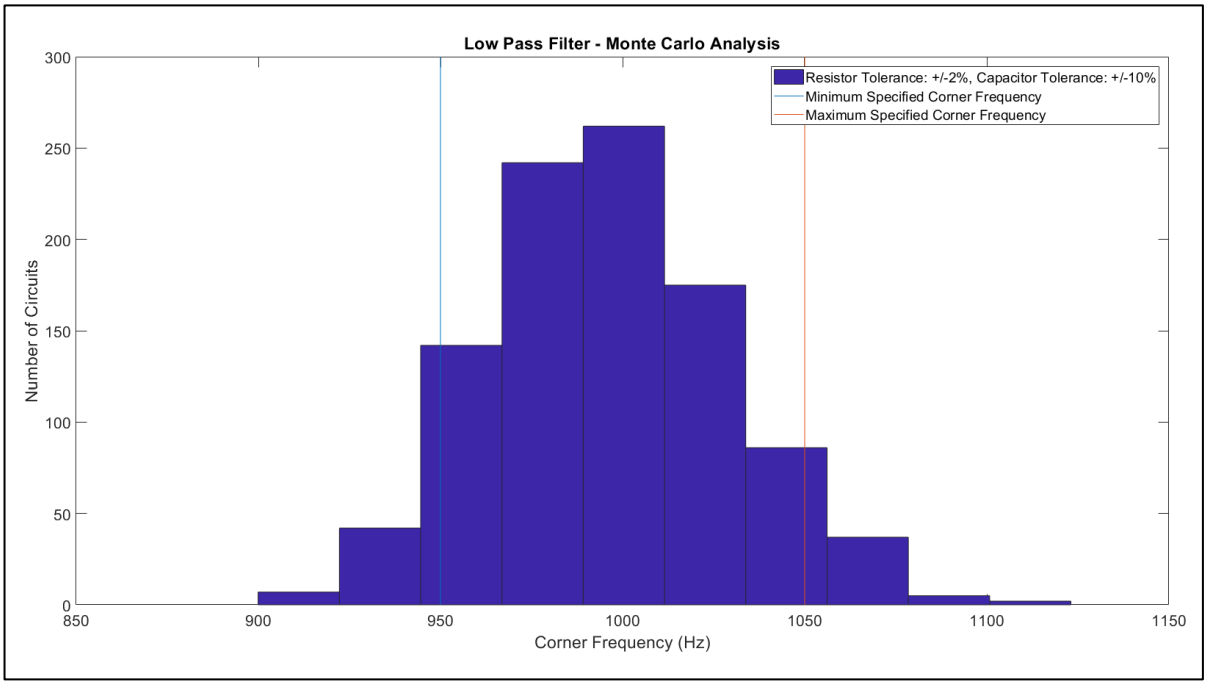

Figure 4.3: Corner Frequency Monte Carlo Analysis - 2% Resistor Tolerance

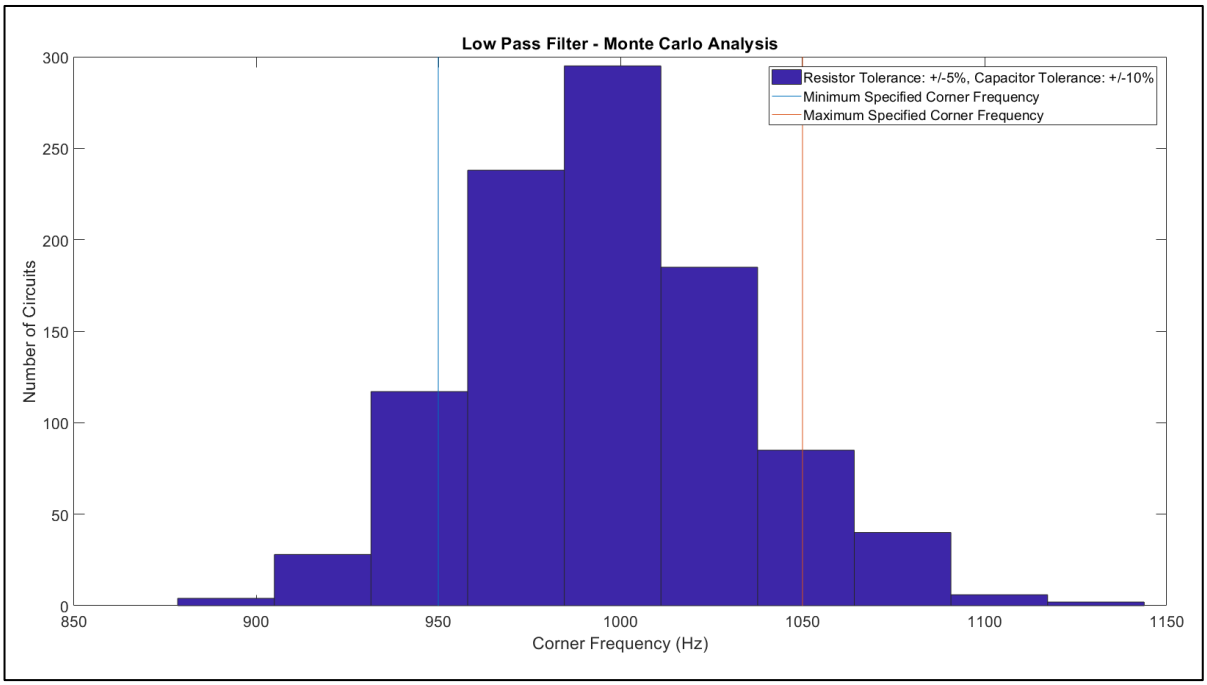

Figure 4.5: Corner Frequency Monte Carlo Analysis - 5% Resistor Tolerance

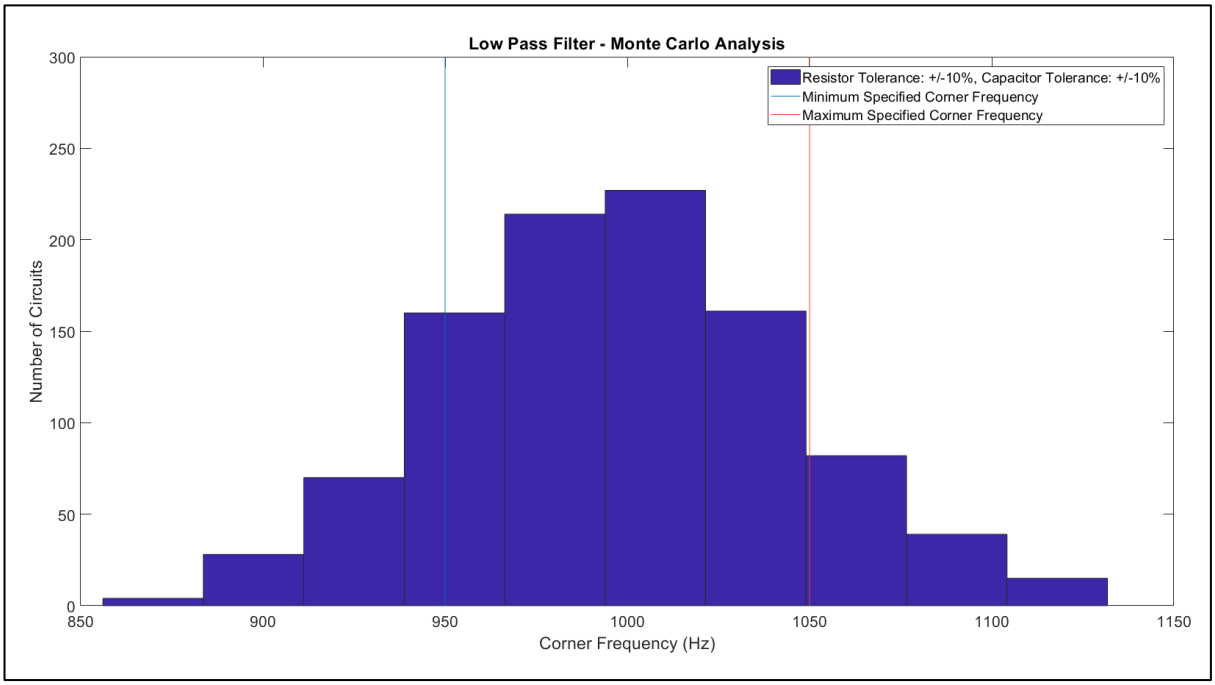

Figure 4.4: Corner Frequency Monte Carlo Analysis - 10% Resistor Tolerance

Figures 4.2 to **4.5** show the same exponential increase in the extreme Corner Frequency values as shown in the Extreme Value Analysis. Again, we can observe that the Monte Carlo Analysis results follow a Gaussian Distribution, although this is to be expected when the Resistor and Capacitor values have been produced using a Gaussian Distribution. This shows us that a higher Yield can be expected than predicted by the Extreme Value analysis as there is a very high probability the Corner Frequency Tolerance will meet the specification even when High values of Tolerance are used for the Resistor and Capacitor values.

These results verify that the results produced by the Extreme Value Analysis, none of the Resistor and Capacitor Tolerance combinations used in **Table 4.2** produce a Corner Frequency Tolerance that satisfies the specification outlined in **Table 4.1** at a Yield of 1. These results are particularly important as high tolerance Capacitors can be very expensive, especially at high values of Capacitance. Where possible it is useful to use Electrolytic Capacitors, which can provide a much higher value of Capacitance at a lower manufacturing cost. Analysis like this can ensure that a circuit will still operate within specification even when an Electrolytic Capacitor is used.

As in **Section 3.2** a graph of Yield was produced using the results from the Monte Carlo Analysis and **Equation 6**. This graph can be seen in **Figure 4.6**.

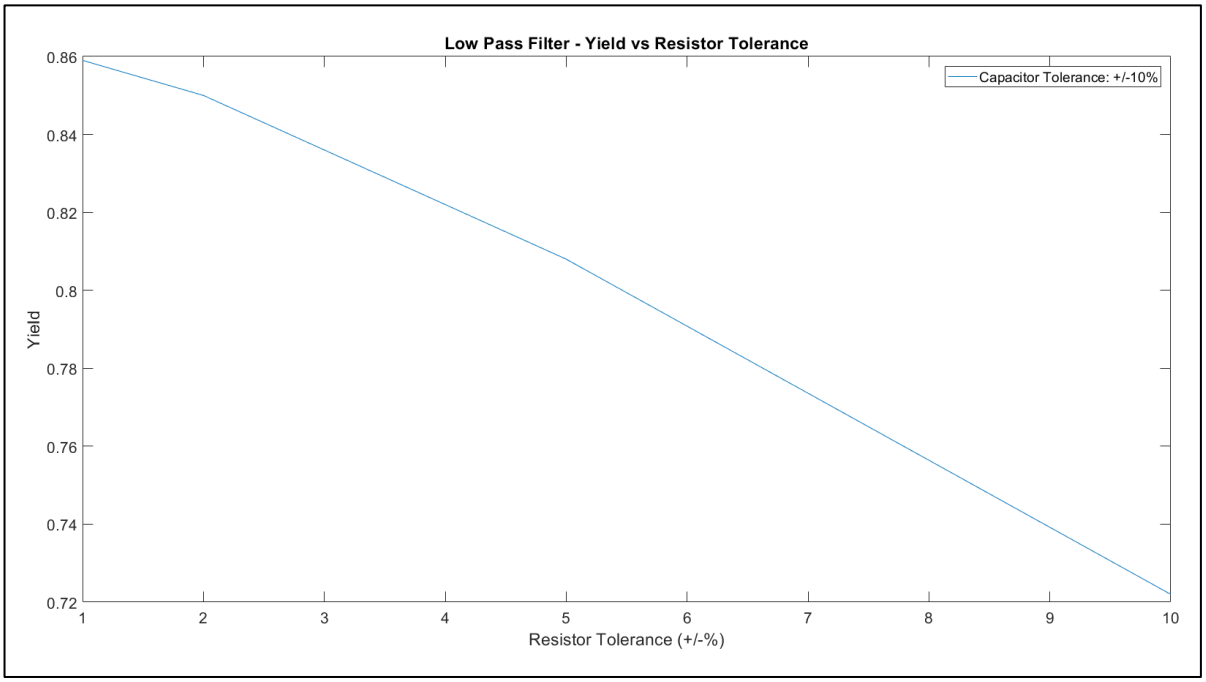

Figure 4.6: Low Pass Filter - Yield vs Resistor Tolerance for 1000 Circuits

Figure 4.6 shows that Yield seems to decrease linearly with Resistor Tolerance. However, if we perform this analysis for a wider range of Resistor Tolerances we can see that the graph of Yield follows an exponential curve, as in **Section 4.2**. Again, this means that very large increases in Yield can be achieved by making small changes to Resistor Tolerance.

4.3 Maximum Capacitor Tolerance

Using the **Equation 10** with a Resistor Tolerance of ±2% and a Corner Frequency Tolerance of ±5% a maximum acceptable value of Capacitor Tolerance was calculated to be approximately ±2%. This value was then verified using a Monte Carlo Analysis of 1000 Circuits using both the Uniform and Gaussian Distributions to randomly generate the Resistor and Capacitor values. The results from these analyses can be seen in **Figure 4.7** and **Figure 4.8** respectively.

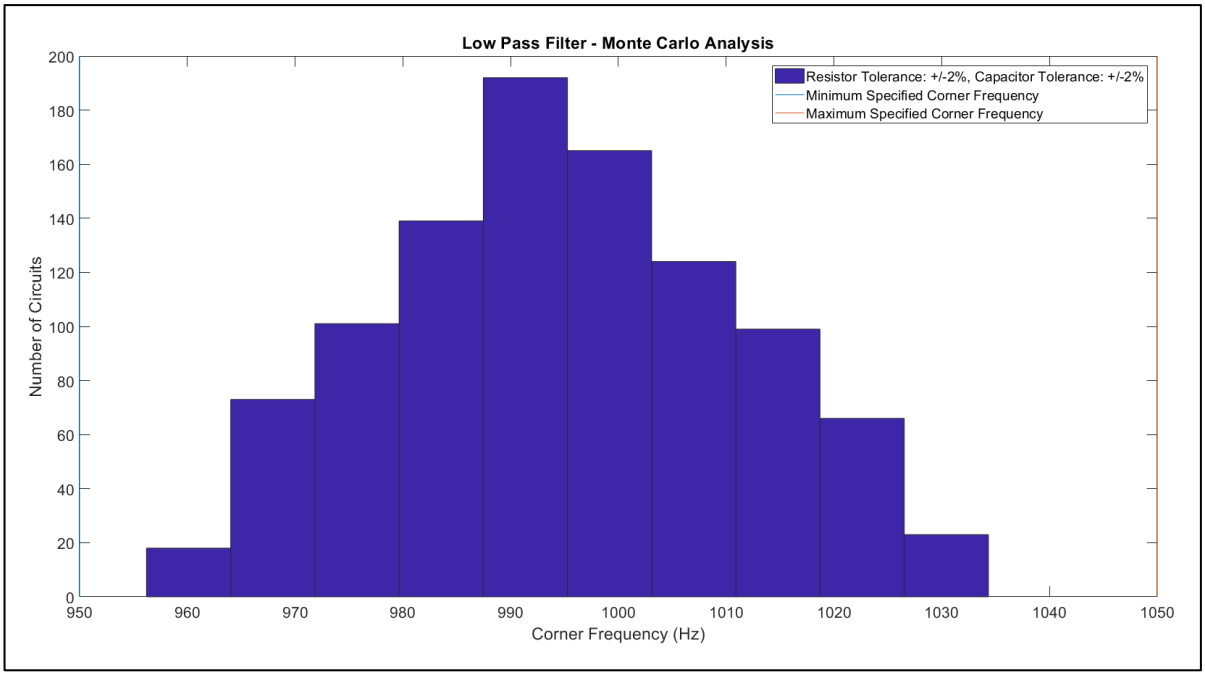

Figure 4.7: Corner Frequency Monte Carlo Analysis - Maximum Value of Capacitance with the Uniform Distribution

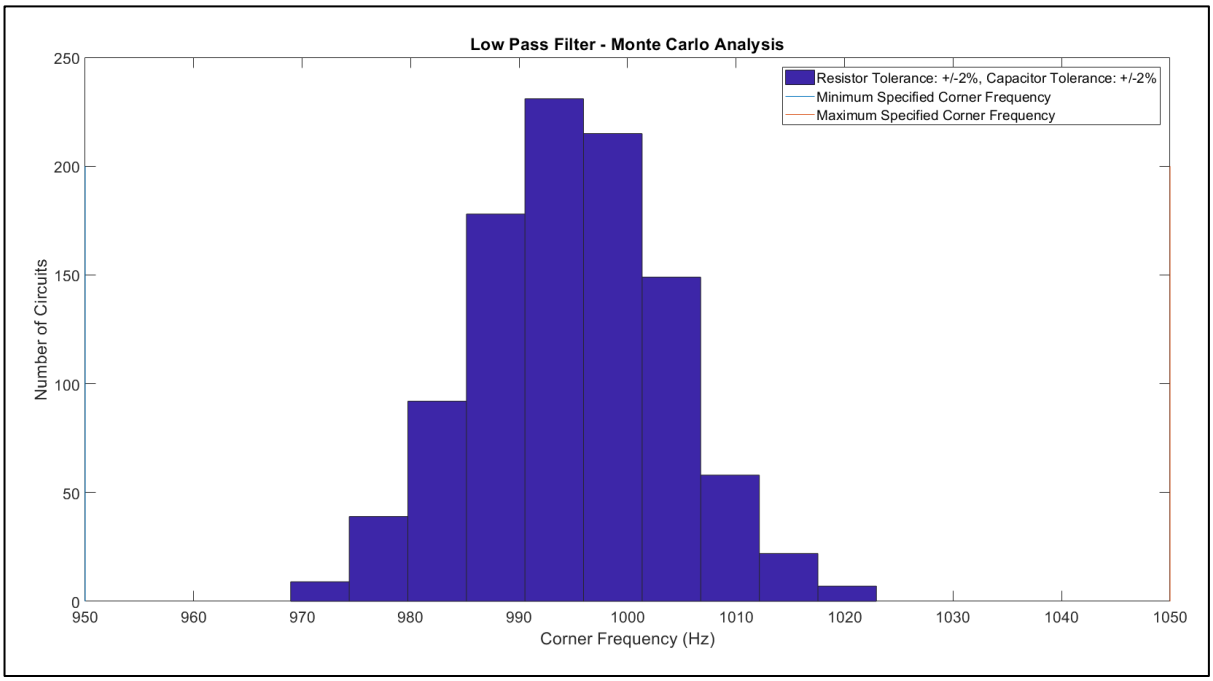

Figure 4.8: Corner Frequency Monte Carlo Analysis - Maximum Value of Capacitance with the Gaussian Distribution

There are two key elements to observe from **Figure 4.7** and **Figure 4.8.** Firstly, we can observe the same effect as was observed in **Section 3.2.** When the Capacitor and Resistor Tolerances are generated using the Uniform Distribution the output Histogram of Corner Frequency approximates to the Gaussian Distribution [1, p. 26] [4]. Again, we can see the origin of this effect in **Equation 8** and **Equation 9.** The probability of the Resistor and Capacitor values both being at the extreme values of their tolerance is much more unlikely than them being moderately away from their nominal value.

Secondly, we can observe that the Histogram produced by the Gaussian distribution generates a smaller range of possible Corner Frequencies than the Uniform Distribution. This is due to the Uniform Distribution making all values of Resistor Tolerance equally likely.

In general, we can show that the tolerance value of ±2% for the Capacitor produces a Yield of 1 for a run of 1000 circuits. However, we can also see that for both probability distributions the Corner Frequencies could have a wider range and still be in specification; by extension therefore, a wider value of Capacitor Tolerance could be used. However, this is a trivial comment as it is impossible to buy specific values of Capacitor Tolerance. Consequently, a value of ±2% Capacitor Tolerance would be used as the first widely available tolerance that meets the Corner Frequency specification.

4.4 Conclusion

In conclusion there are a few key points to take away from this analysis of the Low Pass Filter. Firstly, to meet the specification outlined in **Table 3.1** a tolerance value of ±2% must be used for both the Resistor and Capacitor.

Secondly, we have shown when performing a Monte Carlo Analysis on a Low Pass Filter Circuit with a Gaussian Distribution the output Corner Frequency Histogram also approximates to the Gaussian Distribution with the nominal Corner Frequency as the mean. We have also shown that when performing the same analysis using the Uniform Distribution the Histogram of Corner Frequency can also be approximated to the Gaussian Distribution with the nominal Corner Frequency as the mean.

We have shown that the graph of Yield against Resistor Tolerance for a Low Pass Filter Circuit follows an exponential curve. Thus, large increases in Yield can be achieved with small improvements in Resistor Tolerance.

Finally, we have shown that the range of Corner Frequency values produced by a Monte Carlo Analysis using a Gaussian Distribution is smaller than that produced by the Uniform Distribution. This is due to the Uniform Distribution making every value of Resistor Tolerance within the Tolerance range equally probable. As a result, higher Yields than predicted by the Uniform Distribution may be produced in the real world.

5 Voltage Limiting Circuit

This section outlines the systems design analysis performed on a Voltage Limiting Circuit to determine the circuits behaviour and the effect Resistor Tolerances have on the Maximum Output Voltage of the circuit. Extreme Value and Monte Carlo Analysis were used in conjunction with circuit analysis techniques to produce graphs of the Circuit Output Voltage against a range of parameters. An image of the circuit schematic can be seen in **Figure 5.1**.

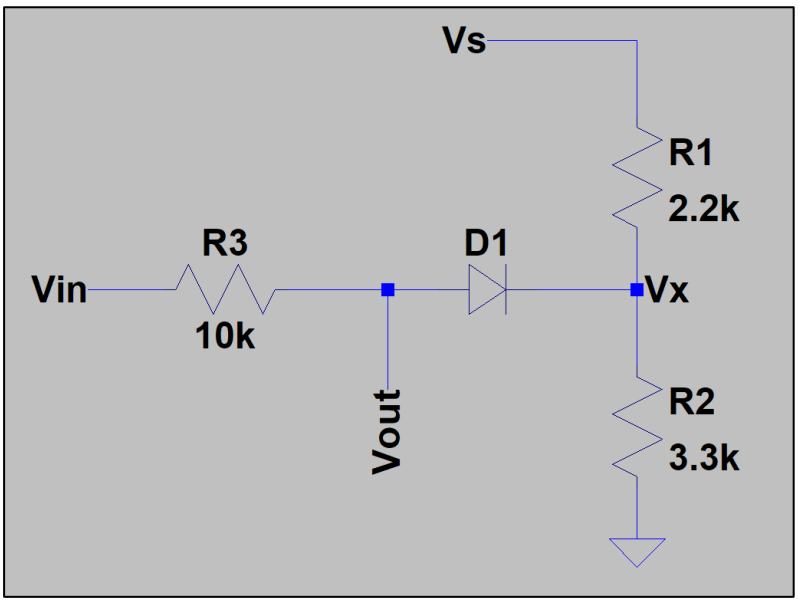

Figure 5.1: Voltage Limiting Circuit [2]

5.1 Input Voltage Limit Expression

To begin analysing the circuit an expression was derived for the Input Voltage Limit ($V_{in(lim)}$); this Voltage defines the point at which the limiting circuit activates and begins limiting the output Voltage. This expression, shown in **Equation 11**, was derived using circuit analysis techniques and the following assumptions:

- The output impedance of the source providing the input signal (V_{in}) is zero.
- The input impedance of the circuit connected to the output voltage (V_{out}) is infinite.
- The Diode D1 is modelled as a switch in series with a voltage source V_d. This diode turns on when the Anode-Cathode voltage is equal to V_d. Once active, the Diode will switch off when the current through it falls to zero.
- The Resistors R1, R2 and R3 have the same tolerance, ΔR.

$$V_{in(\lim)} = V_s \times \frac{R2}{R1 + R2} + V_d \tag{11}$$

5.2 Output Voltage Expression

A circuit analysis was also performed to provide an expression for the Output Voltage (V_{out}) whilst the limiting circuit is active. Again, circuit analysis techniques and the same assumptions from **Section 5.1** where used to derive the expression shown in **Equation 12**.

$$V_{out} = \frac{V_s R2R3 + V_{in} R1R2 + V_d(R1R3 + R2R3)}{R1R3 + R2R3 + R1R2} \tag{12}$$

When the limiting circuit is active, the Output Voltage is controlled by the Potential Divider and the parasitic current that flows through the Diode and into R2. This parasitic current is controlled by the Voltage across R3, which is in turn controlled by the Input Voltage. Consequently, the circuit does not exhibit ideal performance as there will be a slight increase in Output Voltage with Input Voltage even when the circuit is limiting.

5.3 Circuit Specification

As for the previous circuits a specification has been defined to aid with analysis and to give a point to measure circuit performance against. This specification can be seen in **Table 5.1**.

Voltage Limiting Circuit - Specification	
R1	2.2kΩ
R2	3.3kΩ
R3	10kΩ
Supply Voltage (Vs)	5V
Diode Forward Voltage Drop (Vd)	0.7V
Input Voltage (Vin)	5V Amplitude 100Hz Sine Wave
Maximum Acceptable Output Voltage	< 3.9V

Table 5.1: Voltage Limiting Circuit - Specification [2]

5.4 Input Voltage Limit

As specific parameters of the circuit have now been specified in Table 5.1, we can perform calculations using the expressions derived in **Sections 5.1** and **5.2**. The Input Voltage limit was calculated using **Equation 11** to be 3.7V.

5.5 Circuit Output Voltage Plot

To gain an understanding of the operation of the circuit, a plot of the circuit Output Voltage in response to the Input Voltage specified in **Table 5.1** was produced. **Figure 5.2** shows the graph of Output Voltage vs Time for two Input Voltage cycles.

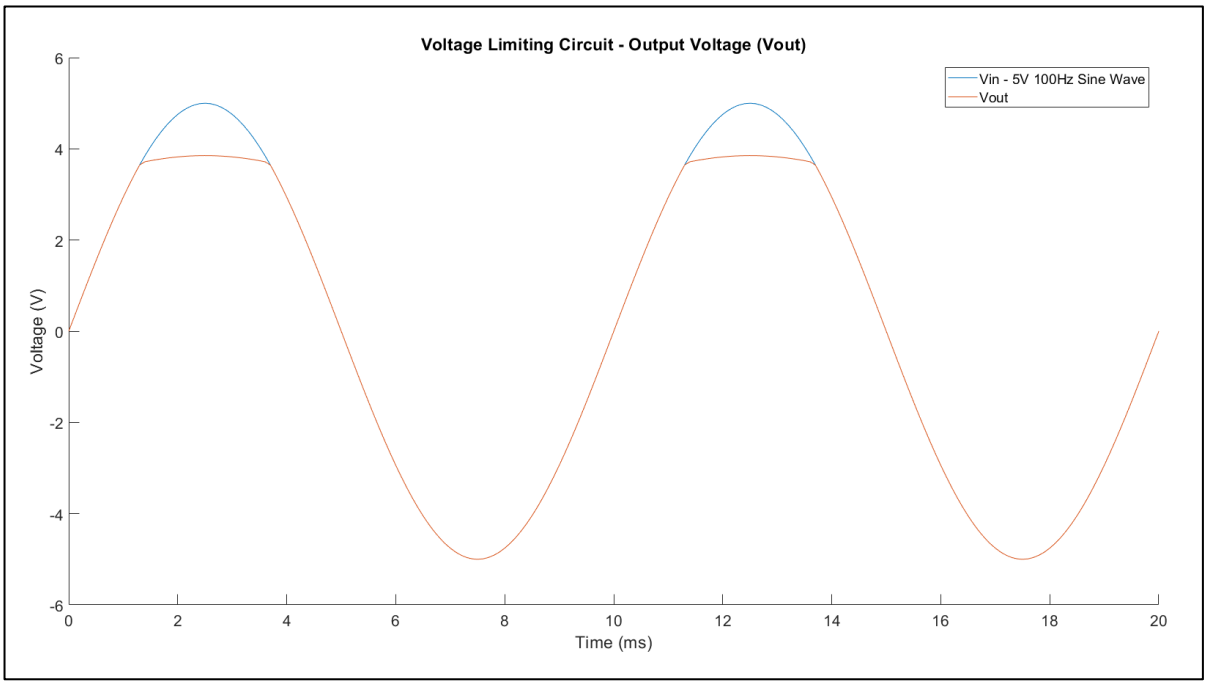

Figure 5.2: Voltage Limiting Circuit Output Voltage in response to a 5V 100Hz Input Sine Wave

On the positive peaks of the Input Voltage we can see that the Output Voltage begins limiting. We can also see the parasitic current causing a slight increase in Output Voltage with Input Voltage as discussed in **Section 5.2**. It is important to note that when using a circuit of this type it is important that the negative peaks of the input signal do cause the Reverse Bias Voltage across the Diode to exceed the Diode Breakdown Voltage as this would cause irreversible circuit failure.

5.6 Maximum Output Voltage

Using the simulation performed in **Section 5.5** and the specification outlined in **Table 5.1** the maximum output voltage of the circuit could be calculated. This was achieved using a MATLAB "max" command on the Output Voltage data from the simulation. The Maximum Output Voltage ($V_{out(max)}$) was calculated to be approximately 3.85V. This is particularly important as we would have to ensure that the circuit we connected V_{out} to was tolerant of this high an Output Voltage.

5.7 Instantaneous Power Dissipation at $V_{out(max)}$

The Instantaneous Power Dissipation in each Resistor was calculated by calculating the Voltage across each resistor and then subbing this value into **Equation 13**.

$$P = \frac{V^2}{R} \tag{13}$$

The calculations produced the following results:

R1: 1.55mW **R2:** 3mW **R3:** 0.132mW

5.8 The Loading effect of R3

By normalising the resistor values to R1 the loading effect of the R3 could be investigated. R3 was normalised using **Equation 14**. R1 and R2 where then normalised using **Equation 15**. **Equation 14** and **15** could then be subbed into **Equation 12** to produce **Equation 16**. **Equation 16** was then used to produce a graph of R3 vs a multiplier of the Output Voltage (V_{out}), this graph can be seen in **Figure 5.3**.

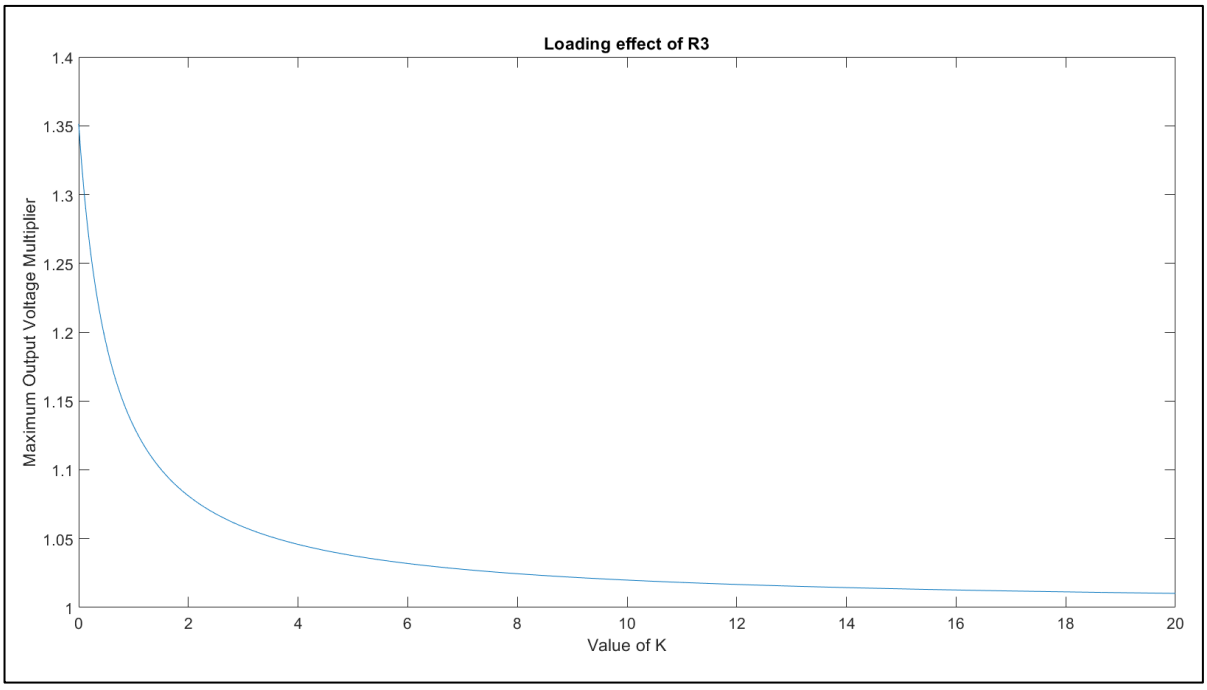

Figure 5.3: Loading Effect of Resistor R3 on the Output Voltage

$$R3 = kR1 \tag{14}$$

$$V_s \times \frac{R2}{R1 + R2} = 1 \tag{15}$$

$$V_{out} = \frac{(V_s k + V_{in}) + V_d k(R1 + R2)}{kR1 + R2(1 + k)} \tag{16}$$

Figure 5.3 shows a behaviour that would be expected when first looking at the circuit. With an increasing value of k (giving an increasing value of R3), the Output Voltage of the circuit tends towards the ideal value of 3.7V when limiting (the voltage set by the Potential Divider). This shows us that ideally this circuit should behave as an ideal analogue building block, with an infinite input impedance and zero output impedance. Consequently, when using this circuit, it is advised that as high a value of resistance be used for R3 to avoid the Output Voltage going out of specification due to parasitic currents.

5.9 Extreme Value Analysis

As in **Sections 3.1** and **4.1** extreme value analysis was performed on the Voltage Limiting Circuit to determine the effect of Resistor Tolerance on the Maximum Output Voltage ($V_{out(max)}$). An expression for the Tolerance in Output Voltage was derived by subbing **Equations 17** and **18** into **Equation 19** along with the specification outlined in **Table 5.1**. This expression can be seen in **Equation 20**. Nominal $V_{out(max)}$ can be calculated using **Equation 21**. It is important to note that ΔR^2 terms were ignored in these equations as their contribution was deemed negligible.

$$Largest\ V_{out(\max)} = \frac{V_s R2R3 + V_{in} R1R2 + V_d R1R3 - 2V_d R1R3\Delta R + V_d R2R3}{R1R3 - 2R1R3\Delta R + R2R3 + R1R2} \tag{17}$$

$$Smallest\ V_{out(max)} = \frac{V_s R2R3 + V_{in} R1R2 + V_d R1R3 + 2V_d R1R3\Delta R + V_d R2R3}{R1R3 + 2R1R3\Delta R + R2R3 + R1R2} \tag{18}$$

$$\Delta V_{out(max)} = \frac{Largest\ V_{out(max)} - Smallest\ V_{out(max)}}{2 \times Nominal\ V_{out(max)}} \times 100 \tag{19}$$

$$\Delta V_{out(max)} = \frac{4.45\Delta R}{2 \times Nominal\ V_{out(max)}} \times 100 \tag{20}$$

$$Nominal\ V_{out(max)} = \frac{V_s R2R3 + V_{in(max)} R1R2 + V_d(R1R3 + R2R3)}{R1R3 + R2R3 + R1R2} \tag{21}$$

Values of 1%, 2%, 5% and 10% Resistor Tolerance were subbed into **Equation 20** to produce the results shown in **Table 5.2**.

Voltage Limiting Circuit - Extreme Value Analysis		
Resistor Tolerance (+/-%)	**Maximum Output Voltage (V 3dp)**	**Meets Specification of <3.9V**
1	3.872	Yes
2	3.895	Yes
5	3.961	No
10	4.073	No

Table 5.2: Voltage Limiting Circuit - Extreme Value Analysis Results

The results from **Table 5.2** show that a maximum Resistor Tolerance of ±2% must be used to ensure that the Voltage Limiting Circuit always meets the specification outlined in **Table 5.1**. As predicted by **Equation 20**, when ignoring ΔR^2 terms the relationship between Maximum Output Voltage Tolerance and Resistor Tolerance is linear.

To wide a Resistor Tolerance could cause one of two eventualities to occur. Firstly, too low a Resistance for R3 could cause too large a parasitic current through the diode, causing the Output Voltage to increase too much with Input Voltage whilst the circuit is limiting. Secondly, the limiting set point $V_{in(lim)}$ controlled by the Potential Divider could be too high, causing the circuit to start limiting when the Output Voltage is above 3.9V.

5.10 Monte Carlo Analysis

As in **Sections 3.2** and **4.2,** to provide a more accurate model of the variation of Resistor Tolerance across a batch of Resistors a Monte Carlo Analysis was performed using **Equation 21**. This analysis was performed on a run of 1000 Circuits using a Uniform Distribution to approximate the variation in Resistor Tolerance. Histograms of Output Voltage were generated using the randomly generated Resistor Values, these Histograms can be seen in **Figure 5.4**, **Figure 5.5**, **Figure 5.6** and **Figure 5.7**.

This Monte Carlo Analysis verifies the results produced by the Extreme Value Analysis, showing that a maximum Resistor Tolerance of ±2% must be used to ensure the Voltage Limiting Circuit has a Yield of 1 when compared to the specification outlined in **Table 5.1**.

Once again, this analysis also confirms that the Histogram produced by a Monte Carlo Analysis using the Uniform Distribution approximates to the Gaussian Distribution, as per the central limit theorem [1, p. 26] [4].

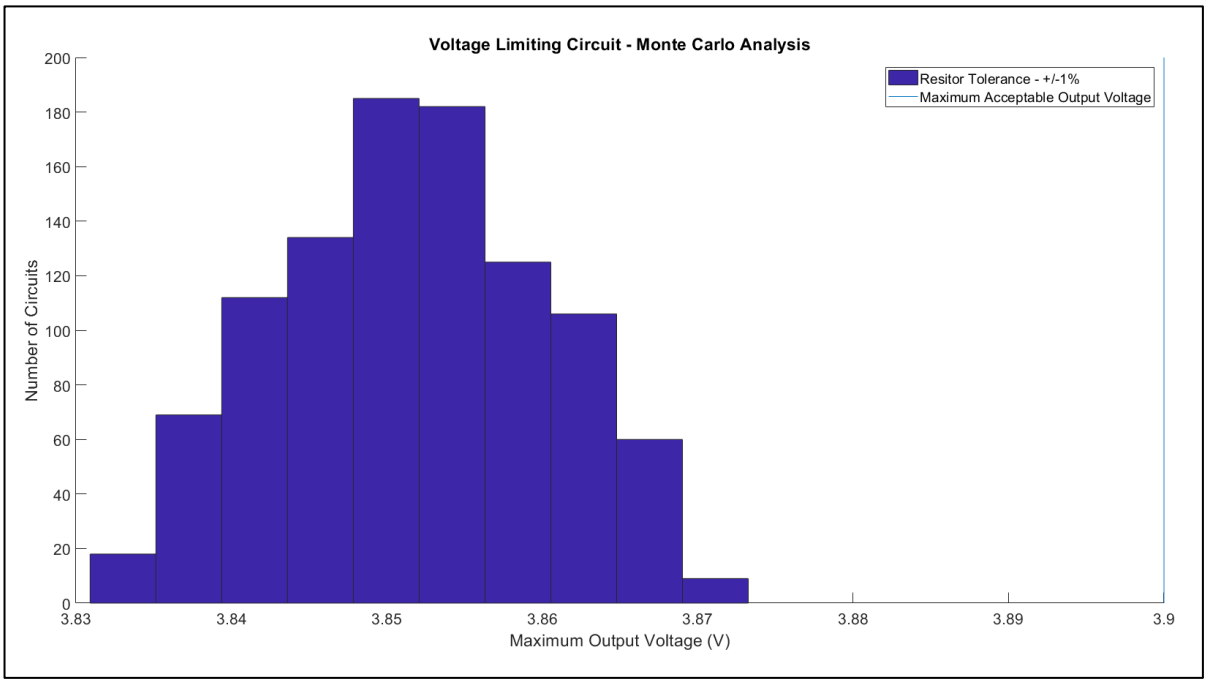

Figure 5.4: Voltage Limiting Circuit Monte Carlo Analysis - 1% Resistor Tolerance

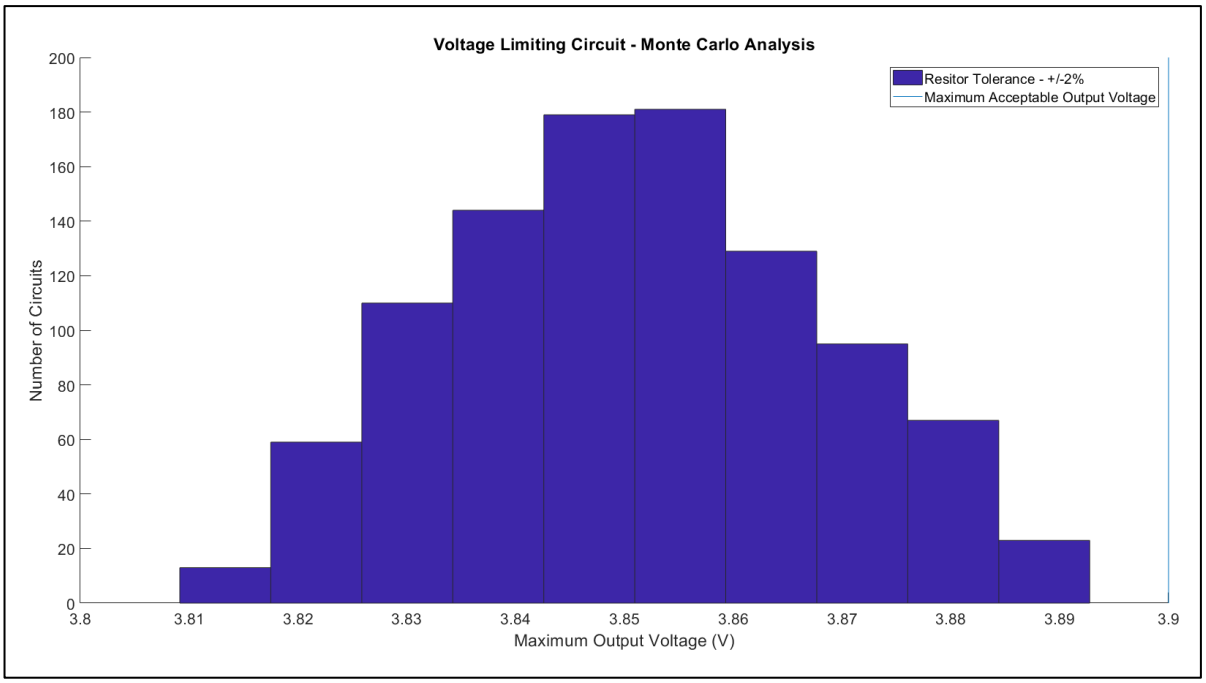

Figure 5.5: Voltage Limiting Circuit Monte Carlo Analysis - 2% Resistor Tolerance

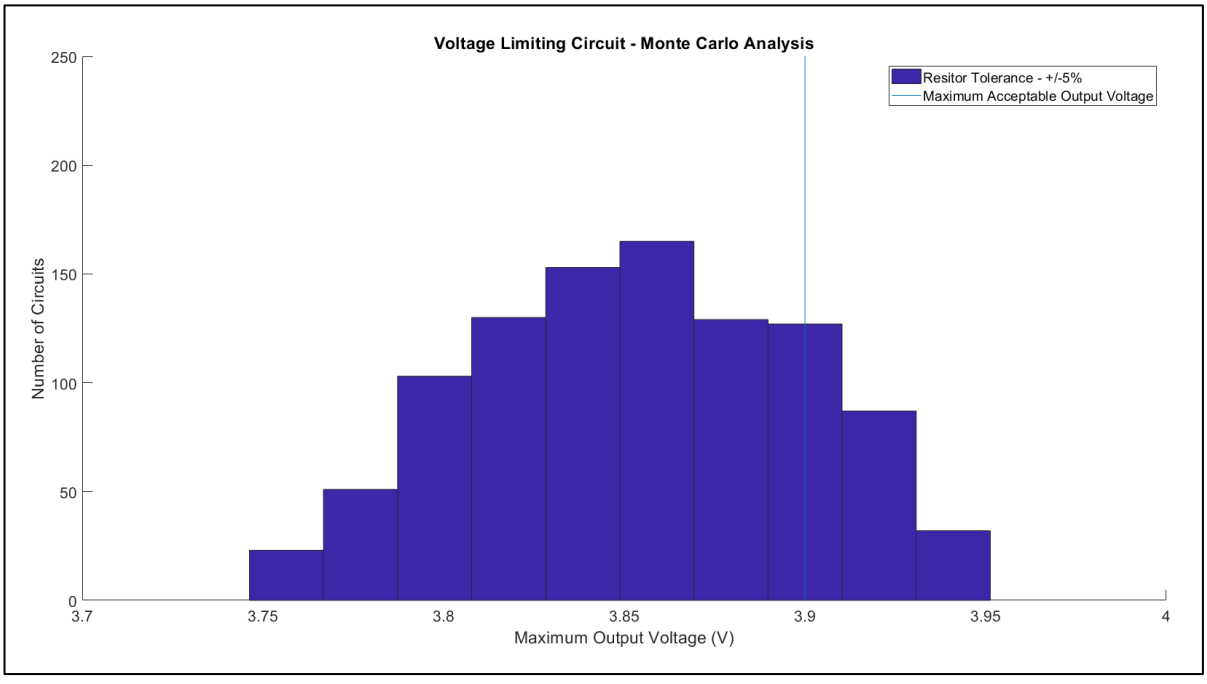

Figure 5.6: Voltage Limiting Circuit Monte Carlo Analysis - 5% Resistor Tolerance

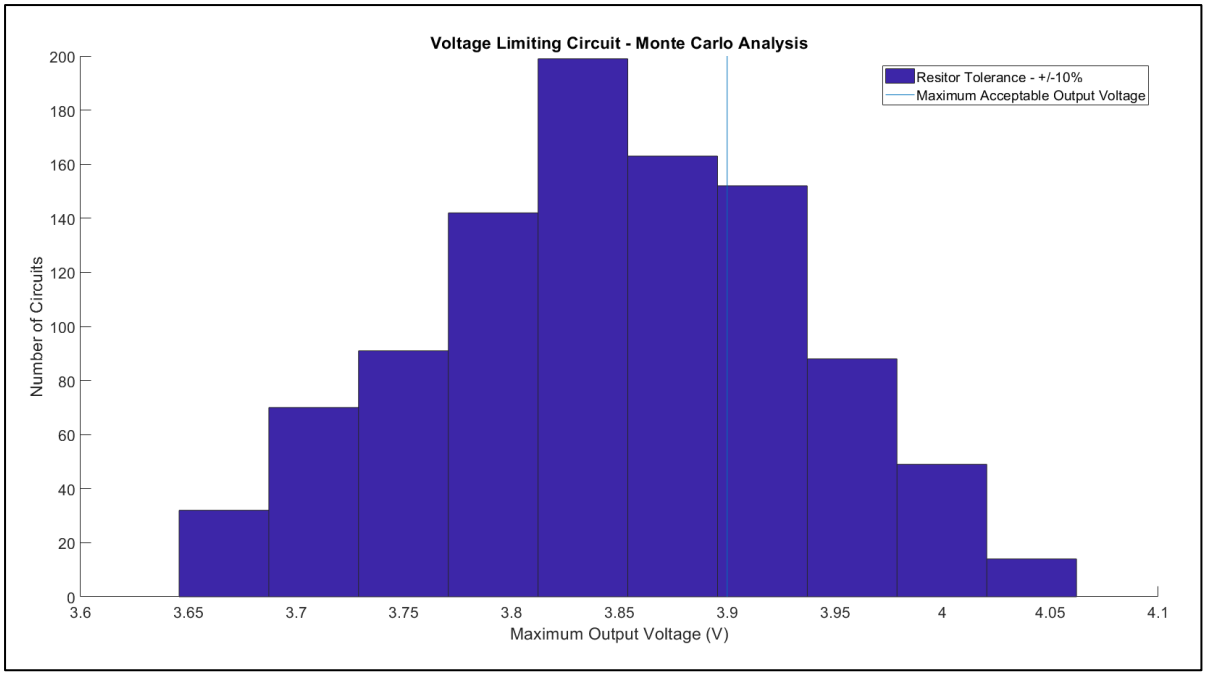

Figure 5.7: Voltage Limiting Circuit Monte Carlo Analysis - 10% Resistor Tolerance

Figure 5.8 shows a graph of Yield vs Resistor Tolerance generated using the data from the Monte Carlo Analysis. This graph confirms the conclusion that ±2% is the maximum Resistor Tolerance that can be used to ensure that the specification outlined in **Table 5.1** is met.

Again, by performing the Yield Analysis over a wider range of Resistor Tolerances we can see that it follows an exponential curve. This has the same implications as described in **Section 4.2**. Achieving maximum Yield is important for this circuit as it ensures the circuitry the Voltage Limiting Circuit is connected to is properly protected. Failure to do this would potentially results in damaging the equipment customers are using.

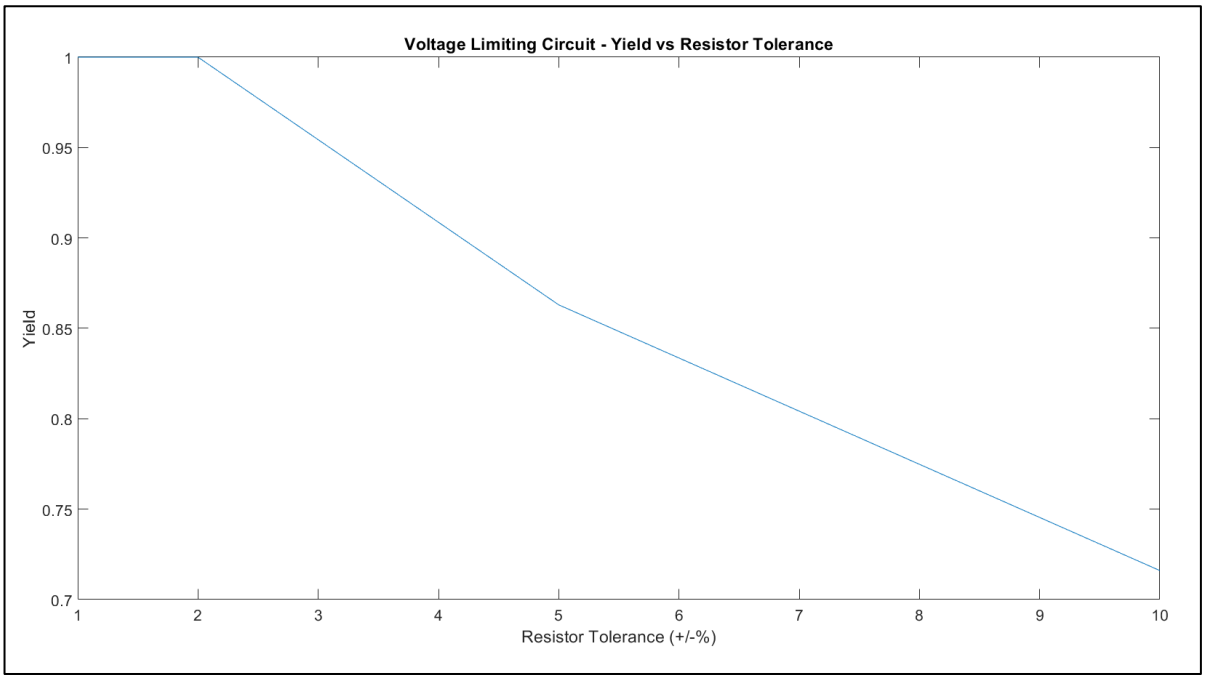

Figure 5.8: Voltage Limiting Circuit - Yield vs Resistor Tolerance

This highlights the importance of practicing proper Systems Design Analysis. If too high a component tolerance was used in the large-scale manufacture of Voltage Limiting Circuits, it could potentially require a large product recall to fix the problem. This would result in extensive expense to the company that could have been avoided with better systems testing and modelling early in the development process.

5.11 Conclusion

In conclusion, we have analysed the operation of a Voltage Limiting Circuit using Circuit, Extreme Value and Monte Carlo Analysis to produce expressions and graphs of different circuit characteristics. This has raised several key points.

For the specification outlined in **Table 5.1** to be met a maximum Resistor Tolerance of ±2% must be used in the manufacture of the circuit. This conclusion is backed up by both the Extreme Value and Monte Carlo Analysis sections **(5.9** and **5.10**) of this report.

We have observed that real world Voltage Limiting Circuits are subject to a parasitic current that flows through the Diode. This causes proportionally linear increase in Output Voltage with Input Voltage when the circuit is limiting. We have also observed that a circuit of this configuration would only be able to limit on the positive peaks of an AC signal.

We have shown that the limiting performance of this circuit can be improved by making the Input Impedance (R3) as high as possible. This acts to limit the parasitic current that flows through the Diode and ensures that the circuit remains within specification over a wide range of voltages.

Monte Carlo Analysis has been used to show verify the results produced by the Extreme Value Analysis. In doing so we have shown that Monte Carlo Analysis of this circuit follows the Central Limit Theorem [1] [4] and thus the Output Voltage can be more easily approximated using the Gaussian Distribution.

Finally, the importance of Systems Design Analysis has been outlined through Yield Analysis. It has been shown that an engineer that fails to perform proper Systems Design Analysis could cause significant cost to a company through circuits that do not always meet specification due to component tolerances.

6 References

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7 Appendices

7.1 MATLAB Code

All graphs in this report were generated using MATLAB. To see the MATLAB code used to generate this data please visit the following link:

Systems Design Assignment - MATLAB Code