Individual Construction Project – Report

1 Introduction

The Individual Construction Project is centred around the construction of an Infrared based Remote Control system to be used in the FYGER competition in place of the current Radio Frequency based system used to control the robots. The system consists of three sections; an Encoder, Modulator and Transmitter; Receiver and Demodulator and a Decoder [1].

The Encoder, Modulator and Transmitter circuit contains an Oscillator, Infrared LED Driver and Infrared LED; this circuit is used to generate and transmit a signal that indicates which one of four control buttons has been pressed [1].

The Receiver and Demodulator circuit consists of a photodiode, tuned amplifier stages and a peak detector demodulation stage [1]. Tuned amplifier stages are used to ensure only a specific carrier frequency is detected by the receiver circuit. This allows a carrier frequency to be selected for each robot, ensuring that multiple robots can be controlled within a race without interference between different robot controls.

The Decoder circuit consists of a Decoder IC that converts the digital signal produces by the demodulator stage into a selection of one of four digital output lines [1]. These output lines can be used to control different sections of the robot.

The aim of the Individual Construction Project is to successfully construct, test and verify the Receiver and Demodulator circuit.

2 Theory

2.1 First Stage – Tuned Folded Cascode Amplifier (TP1 to TP2)

Carrier Frequencies were allocated based upon Surname or Family name [1], thus the selected Carrier Frequency for my Receiver and Demodulator circuit was 71kHz. **Figure 1** shows the First Stage Tuned Folded Cascode Amplifier (TP1 to TP2); L1, R9 and C12 set the Resonant Frequency and Bandwidth of the Amplifier. The value of C12 was given along with the Carrier Frequency as 470pF, **Equation 1** was then used to calculate the value of L1 based upon the Resonant Frequency of 71kHz.

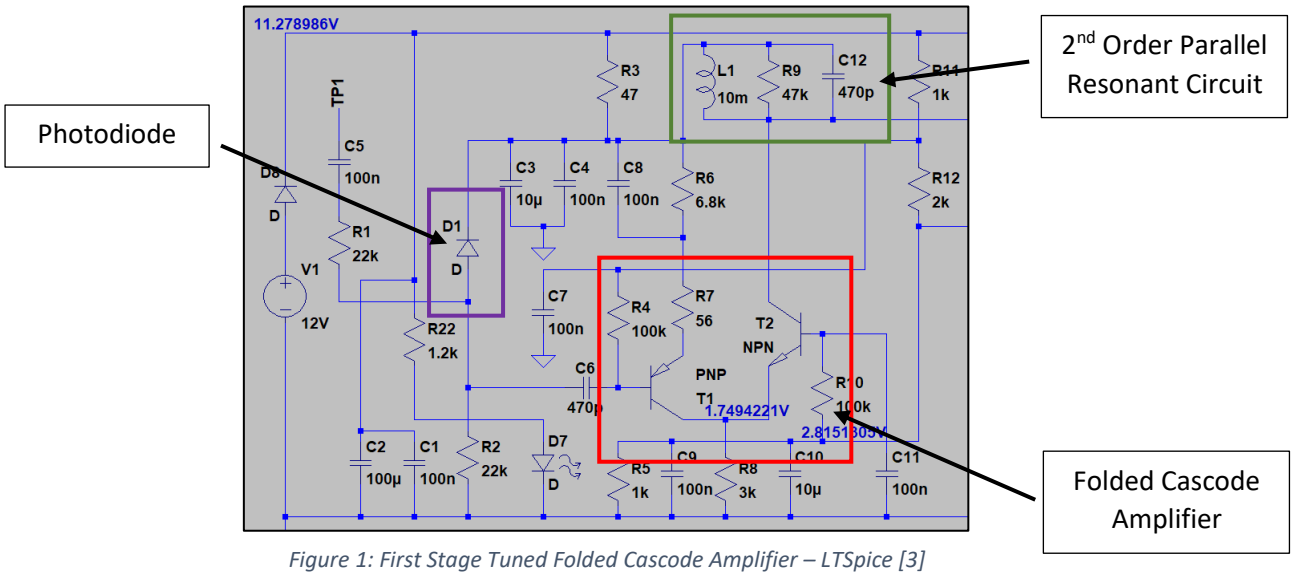

Figure 1: First Stage Tuned Folded Cascode Amplifier – LTSpice [3]

$$L = \frac{1}{4\pi^2 {f_r}^2 C} \quad (1)$$

$$Q = \frac{f_r}{f_b} \quad (2)$$

$$R = Q\sqrt{\frac{L}{C}} \quad (3)$$

For this specific circuit the value of L1 was calculated to be 10mH (when selecting from available inductance values [1]). **Equation 2** [2, p. 53] was used to calculate the Quality Factor (Q) based upon the specified Resonant Frequency (f_r) of 71kHz and Bandwidth (f_b) of 7.5kHz. **Equation 3** [2, p. 53] was then used to calculate the value of R9 required to satisfy the calculated Q Factor of 9.47; R9 was given a value of 47kΩ (when selecting from the E12 series of resistors [1]).

2.2 Second Stage – Tuned Cascode Amplifier (TP2 to TP3)

Figure 2 shows the Second Stage Tuned Cascode Amplifier (TP2 to TP3). Using the same method as for the First Stage, the values of L2, C15, R15 and R16 were calculated to create the 2nd Order Parallel Resonant Circuit that tunes the Second Stage Amplifier. **Equation 1** [2, p. 53] gave a value of 3.3mH for L2 from a specified value of 1.5nF for C15. Using the Q Factor of 9.47 previously calculated using **Equation 2**, the values for R15 and R16 were calculated using **Equation 3**. R15 and R16 are effectively in parallel for AC signals, consequently the parallel combination of R15 and R16 must equal the value given by **Equation 3**. For this specific circuit R15 and R16 were given values of 30kΩ.

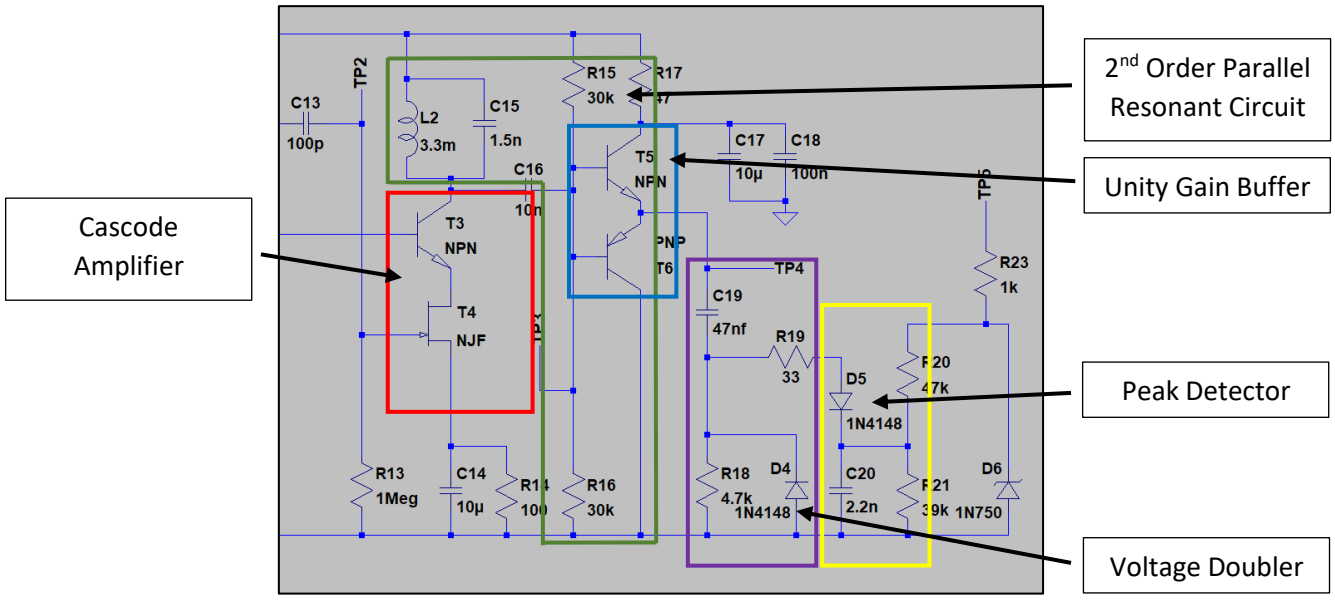

Figure 2: 2nd to 4th Stage of Receiver and Demodulator Circuit

2.3 Third Stage – Push Pull Unity Gain Buffer (TP3 to TP4)

Figure 2 shows the Push Pull Unity Gain Buffer between TP3 and TP4. This buffer is in place to ensure that the gain of the First and Second stage amplifiers is not affected by the load of the Demodulator circuit, and to provide the voltages and currents required by the Demodulator via C17 and C18.

R15 and R16 provide the DC set point for the Buffer; to provide maximum voltage swing R15 and R16 are set to the same value to place the DC set point at exactly halfway between the Voltage Rails. As stated previously R15 and R16 were given a value of 30kΩ.

2.4 First and Second Stage Gain

To verify the operation of the circuit during testing the theoretical gain of stages one and two was calculated using **Equation 4** [1] and **Equation 5** [1]. The linear sum of these values can then be used to calculate the total gain of stages one and two.

$$first\ stage\ gain \approx 20 \times \log_{10}(2.0 \times 10^{-3} \times R9 \times \frac{jf/(f_r Q)}{1 - \left(\frac{f}{f_r}\right)^2 + j\frac{f}{f_r Q}}) \quad (4)$$

$$second\ stage\ gain \approx 20 \times \log_{10}(4.5 \times 10^{-3} \times \frac{R15 \times R16}{R15 + R16} \times \frac{jf/(f_r Q)}{1 - \left(\frac{f}{f_r}\right)^2 + j\frac{f}{f_r Q}}) \quad (5)$$

These equations, at resonance, gave the following results for the gain of the amplification stages:

First Stage Gain: 39.5 (1dp)

Second Stage Gain: 36.6 (1dp)

Combined First and Second Stage Gain: 76.1 (1dp)

2.5 Fourth Stage – Demodulator (TP4 to TP5)

It is important to note that the demodulator stage required no calculations as all values were already pre-defined in the circuit schematic. The values of Capacitors C19 and C20 and Resistors R18, R20 and R21 have been carefully selected to ensure the voltage doubler and peak detector respond to all potential carrier frequencies correctly.

3 Results

This section aims to show how the performance of the complete real-world circuit compares to the theoretical responses obtained from **Equations 1 – 5** and LTSpice [3] simulations. The process of testing and verification is shown along with the responses of the circuit across key stages.

3.1 First Stage – Tuned Folded Cascode Amplifier (TP1 to TP2)

A simulation of the response of the first stage to a 25mVpp 71kHz Sine Wave injected at TP1 was performed to see what the theoretical performance of the system was, this can be seen in **Figure 3**. **Equation 4** was also used to produce a frequency vs gain graph for the First Stage, this can be seen in **Figure 5**.

Once the circuit was constructed it was tested using the same 25mVpp 71kHz Sine Wave to see if the response compared well to the results of the simulation. The oscilloscope capture of the First Stage response can be seen in **Figure 4**. Finally, a frequency response graph was produced using a 25mVpp Sine Wave at a range of frequencies as an input signal, this can also be seen in **Figure 5**.

For all practical tests, a Keysight 33500B Function Generator was used in conjunction with a Keysight MSO-X-2012A Oscilloscope to produce the results; a Keysight UU8031A DC PSU was used to provide the main 12V supply for the circuit board. Oscilloscope Channel 2 was used to display the output.

The results for the graph in **Figure 5** can be seen in **Table 1** in the Appendices.

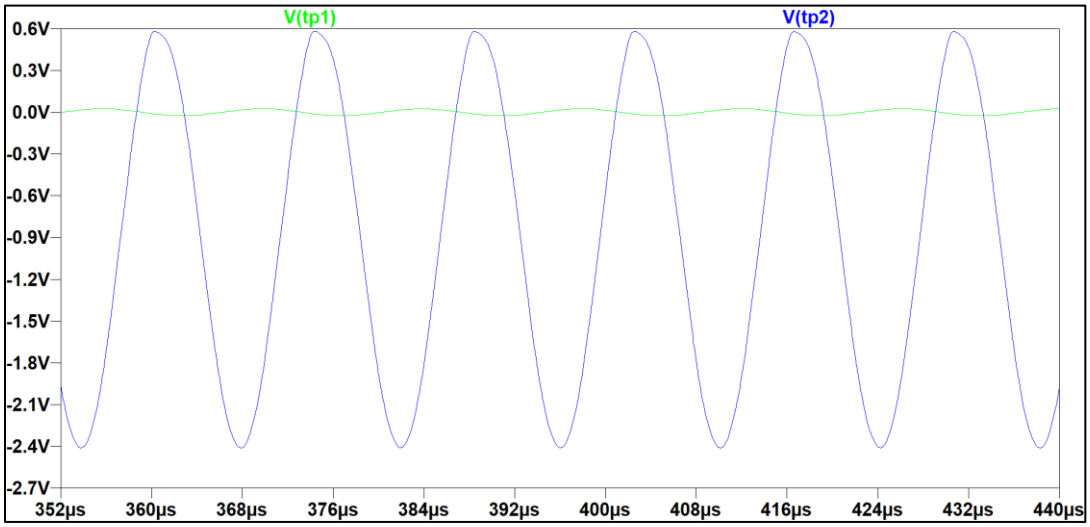

Figure 3: Theoretical First Stage response to a 25mVpp 71kHz Sine Wave – Generated with LTSpice [3]

Figure 4: Actual First Stage response to a 25mVpp 71kHz Sine Wave

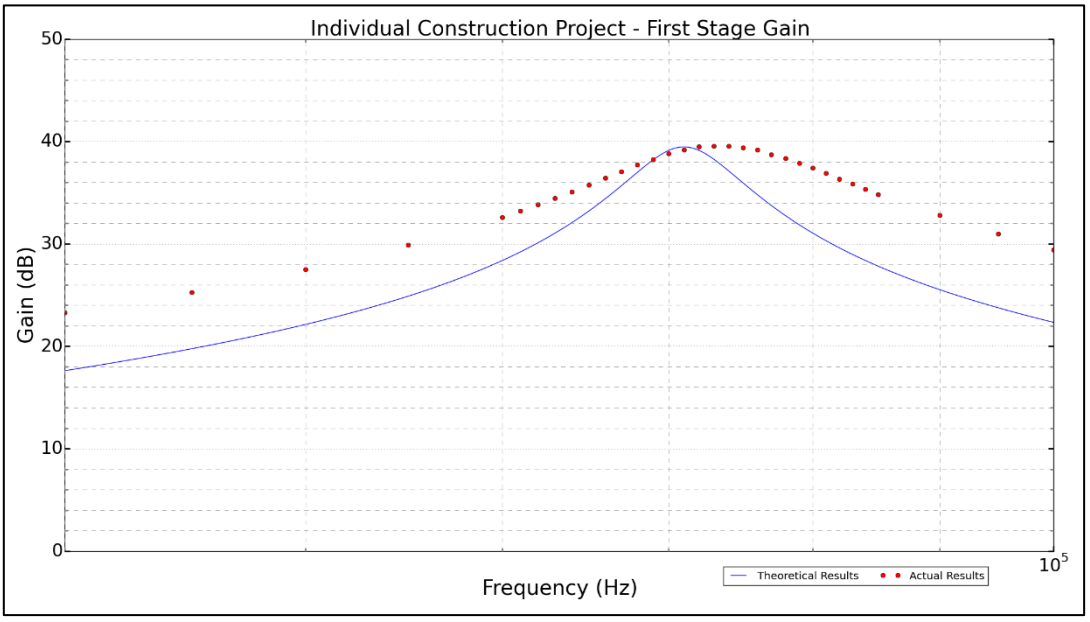

Figure 5: Theoretical and Actual First Stage Frequency Response – Generated with Python XY [4]

The Resonant Frequency of Stage One was set to have a theoretical value of 71kHz, as discussed in **Section 2.1. Figure 5** shows the theoretical values of gain compared to the actual values of gain produced by the First Stage Folded Cascode Amplifier. We can see that the actual Resonant Frequency of the actual Folded Cascode Amplifier Resonant Circuit is approximately 73kHz.

The Quality Factor of Stage One was set to have a theoretical value of 9.47, as discussed in **Section 2.1.** Again, the actual value of Quality Factor can be taken from **Figure 5.** We can see that the actual Quality Factor of the Folded Cascode Amplifier Resonant Circuit is approximately 4.87.

3.2 Second Stage – Tuned Cascode Amplifier (TP2 to TP3)

A simulation of the response of the Second Stage to a 25mVpp 71kHz Sine Wave injected at TP1 was produced using LTSpice [3], this can be viewed in **Figure 6**. A Theoretical Frequency Response to a 25mVpp Sine Wave was also generated using **Equation 5** and Python XY [4], this can be seen in **Figure 8**.

Again, once the circuit was constructed it was tested using the same 25mVpp 71kHz signal injected at TP1, the response can be seen in **Figure 7**. A Frequency Response graph was also generated using a 25mVpp signal injected into TP2 at varying frequencies, the results from this test can be seen in **Figure 8**. The same equipment as described in **Section 3.1** was used during these tests. The results for the graph in **Figure 8** can be seen in **Table 2** in the Appendices.

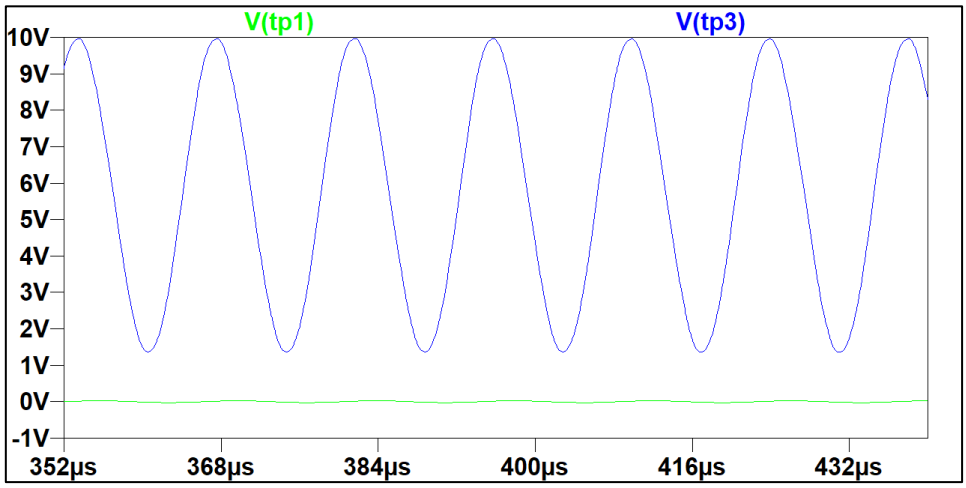

Figure 6: Theoretical Second Stage Response to 25mVpp 71kHz Sine Wave - Generated using LTSpice [3]

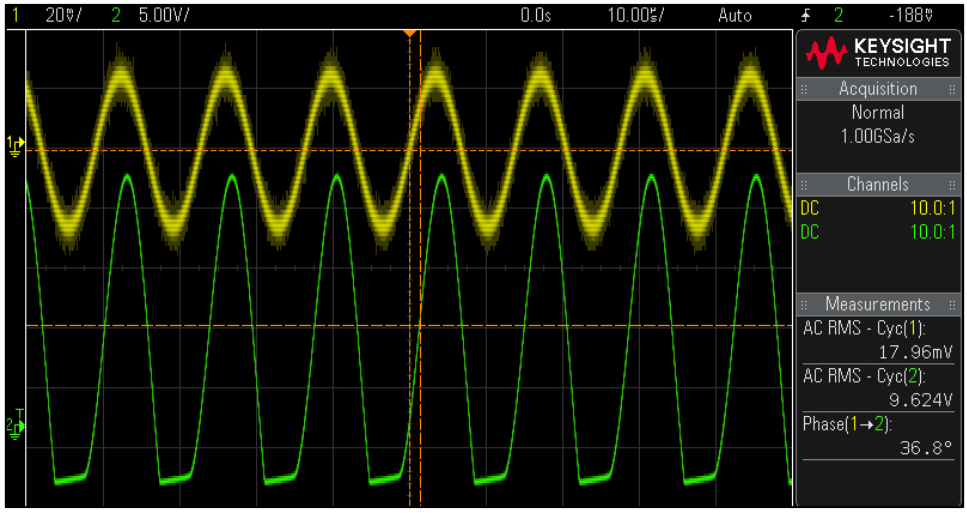

Figure 7: Actual Second Stage Response to 25mVpp 71kHz Sine Wave

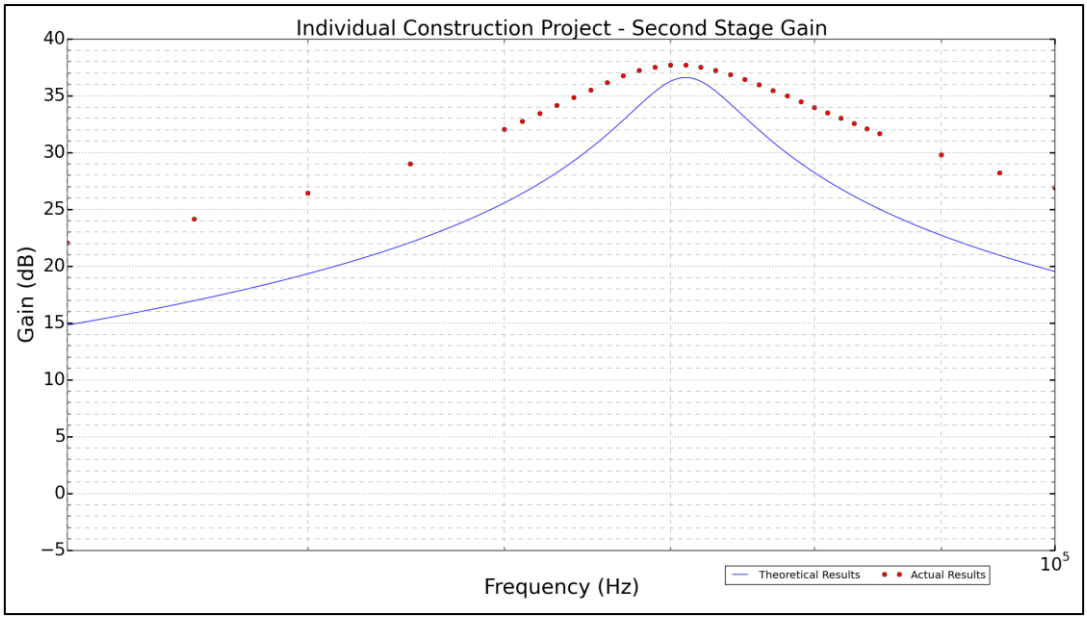

Figure 8: Theoretical and Actual Second Stage Frequency Response – Generated using Python XY [4]

The Resonant Frequency of the resonant circuit used to tune the Second Stage Cascode Amplifier was also set to 71kHz, as discussed in **Section 2.2**. **Figure 8** shows the theoretical values of gain compared to the actual values of gain produced by the Second Stage Cascode Amplifier. We can see that the Resonant Frequency of the actual Cascode Amplifier Resonant Circuit is approximately 70.5kHz.

The Quality Factor of Stage Two was set to have a theoretical value of 9.47, as discussed in **Section 2.2.** Again, the actual value of Quality Factor can be taken from **Figure 8,** which shows that the Quality Factor of the actual circuit is approximately 5.22.

3.3 Third Stage – Push Pull Unity Gain Buffer (TP3 to TP4)

A simulation of the response of the Third Stage to a 25mVpp 71kHz Sine Wave injected at TP1 was produced using LTSpice [3], this can be seen in **Figure 9**. Once constructed the circuit was tested using the same signal, the actual response can be seen in **Figure 10**.

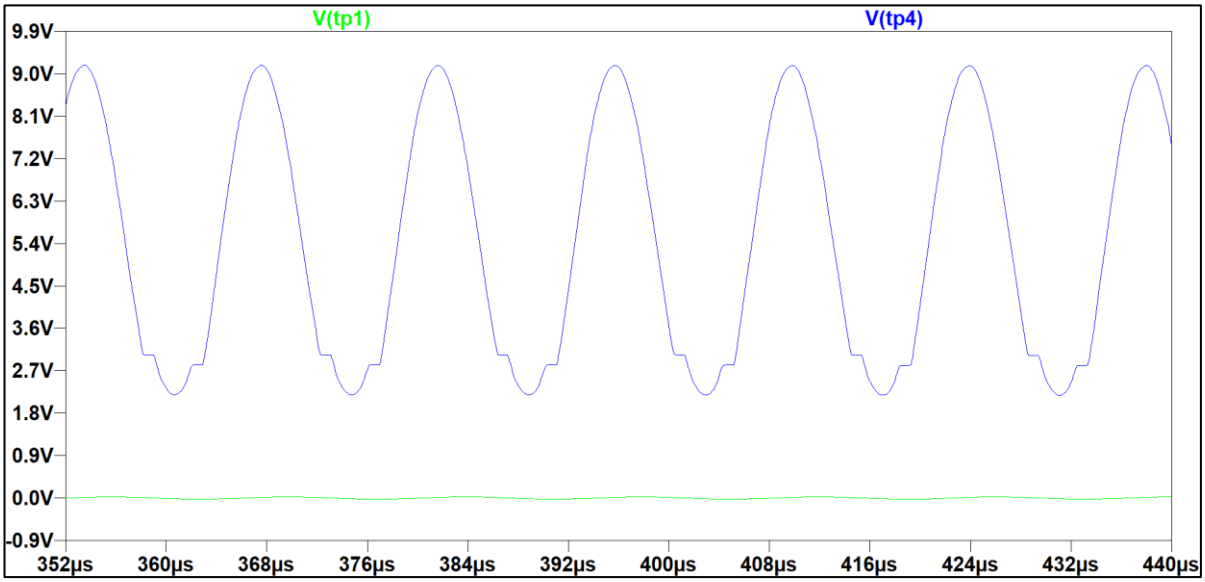

Figure 9: Theoretical Third Stage Response to 25mVpp 71kHz Sine Wave - Generated using LTSpice [3]

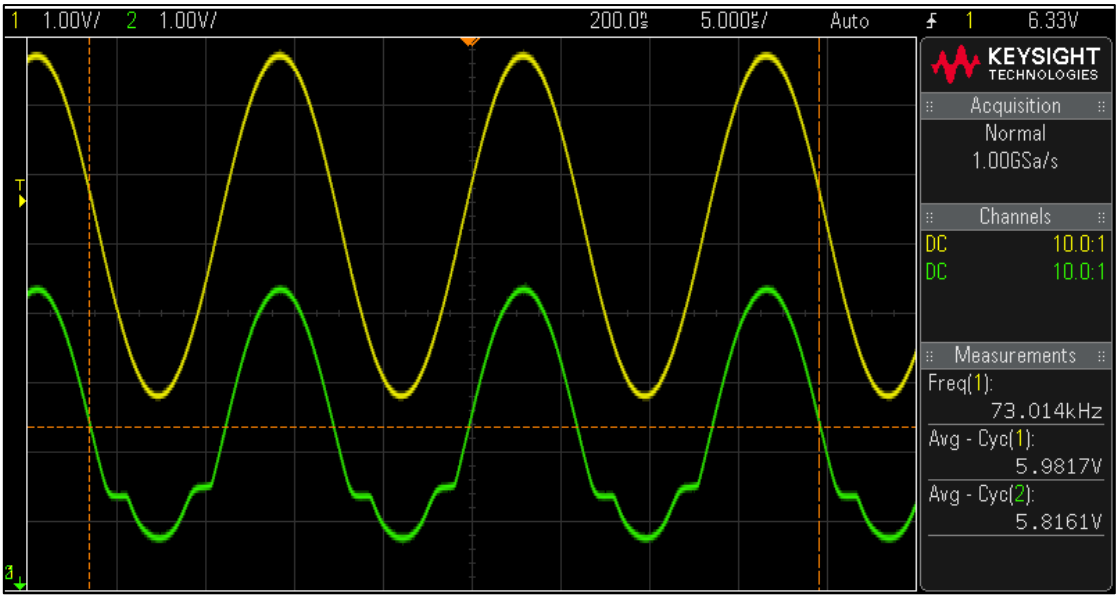

Figure 10: Actual Third Stage Response to 25mVpp 71kHz Sine Wave

3.4 Fourth Stage – Demodulator (TP4 to TP5)

A simulation of the response of the Fourth Stage to a 25mVpp 71kHz Sine Wave injected at TP1 was produced using LTSpice [3], the output of the Peak Detector was measured; this can be seen in **Figure 11**. Once constructed the circuit was tested using the same signal, measuring the output of the Peak Detector; this can be seen in **Figure 12**.

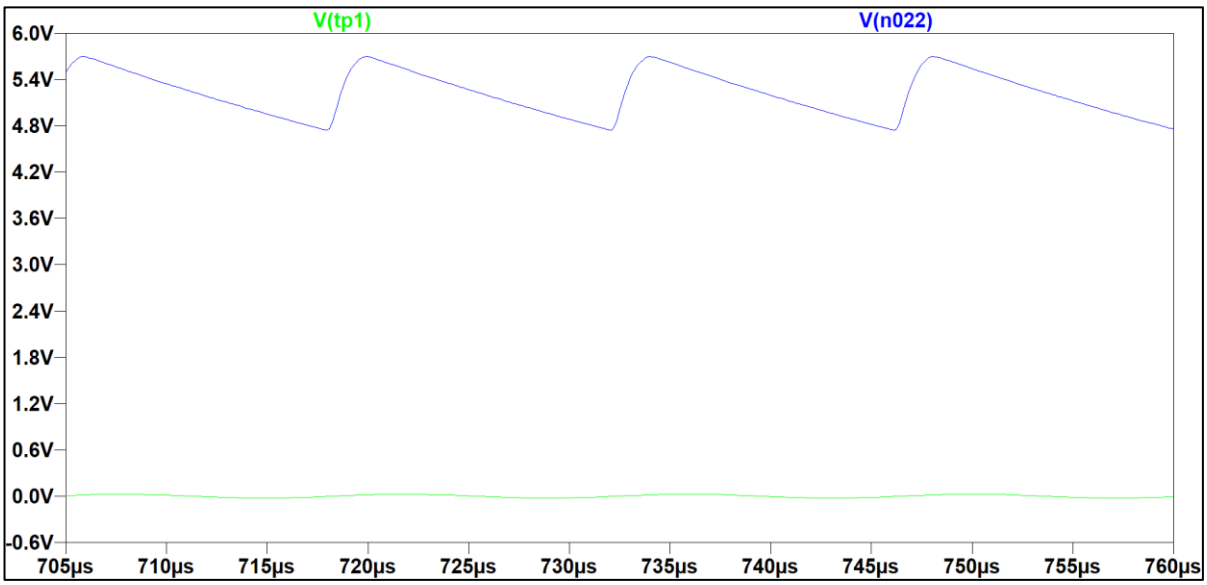

Figure 11: Theoretical Peak Detector Response to 25mVpp 71kHz Sine Wave - Generated with LTSpice [3]

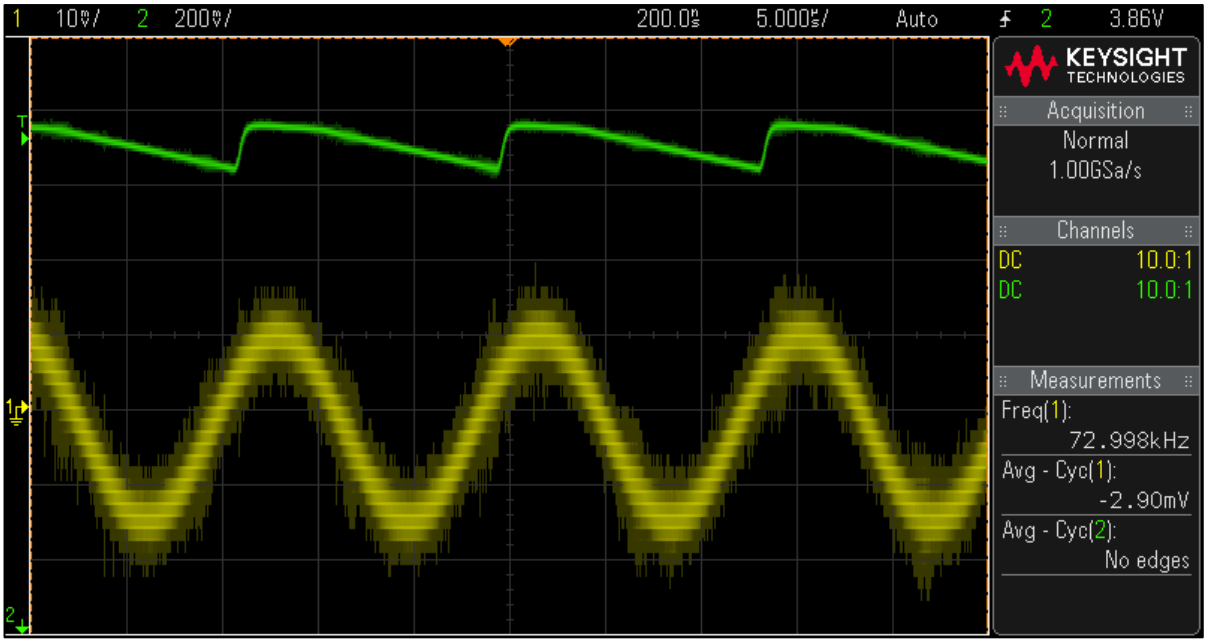

Figure 12: Actual Peak Detector Response to 25mVpp 71kHz Sine Wave

4 Discussion

This section aims to analyse and discuss the results presented in **Section 3**. Attempts will be made to explain the differences between theoretical and actual results. Comparing **Figures 3, 6, 9** and **11** to **Figures 4, 7, 10** and **12** we can see that the circuit is functioning as intended. The real-world results compare favourably to the simulation outputs for all stages.

4.1 First Stage – Tuned Folded Cascode Amplifier (TP1 to TP2)

The results produced by the simulation of the First Stage response shown in **Figure 3** compare very closely to the actual results shown in **Figure 4**. The theoretical results show a slightly larger negative DC offset compared to the actual results, there is also more distortion shown in the positive peaks of the theoretical results. This will largely be due to the differences in the characteristics used in the LTSpice Transistor model compared to the real-world characteristics of the BC212L and BC183L Transistors. However, the gain of the actual stage at resonance is very similar to the gain of the simulated stage at resonance, with both peaking at a gain of approximately 39.5 (**Figure 5**).

However, **Figure 5** shows large differences are present between the theoretical and real-world performance of the 2nd Order Resonant Circuit used to tune the amplifier to a Resonant Frequency of 71kHz and a Quality Factor of 9.47. The actual resonant frequency is closer to 73kHz and the Quality Factor has an approximate value of 4.87. This results in the circuit having a wider than ideal bandwidth, making the possibility of cross talk with nearby carrier frequencies more likely. It is likely this is caused by a parasitic resistance in the circuit causing the impedance of the Resonant Circuit to be mostly resistive, thus making its impedance much more independent of frequency. As well as the actual component values not being the same as those calculated using **Equations 1 to 3.**

4.2 Second Stage – Tuned Cascode Amplifier (TP2 to TP3)

The results generated by the simulation of the Second Stage response shown in **Figure 6** compare very closely to the actual results shown in **Figure 7**. The theoretical results show no distortion on the negative troughs of the signal; the peak to peak voltage swing is also 8.5V as opposed to the approximate 25V shown in the actual results. This shows that the actual circuit has a higher gain than the simulation. This is reflected in the frequency response graph (**Figure 8**) which shows the actual amplifier reaching a peak gain of approximately 38 as opposed to the predicted 36.5.

However, **Figure 8** shows a large difference between the theoretical and actual frequency response of the Resonant Circuit used to tune the Cascode Amplifier to a Resonant Frequency of 71kHz and a Quality Factor of 9.47. The actual resonant frequency is approximately 70.5kHz and the Quality Factor has an approximate value of 5.22. Again, this results in circuit having a wider than ideal bandwidth, making the possibility of cross talk with other carrier frequencies more likely. Once more this is due to the parasitic resistances of the components and the difference between the calculated and actual component values due to manufacturing tolerances.

4.3 Third Stage – Push Pull Unity Gain Buffer (TP3 to TP4)

A brief comparison of **Figure 9** and **Figure 10** shows that Stage Three is functioning correctly. Both the theoretical and actual signals show similar distortion at the troughs due to transistor switching, they also have a similar DC offset of approximately 5.6V – 6V.

4.4 Fourth Stage – Demodulator (TP4 to TP5)

A brief comparison of **Figure 11** and **Figure 12** shows that Stage Four is functioning correctly. Both the theoretical and actual signals show a very similar sawtooth waveshape. However, the actual circuit shows a much lower ripple voltage than the simulation, as well as a lower DC offset. This will be due to the lower peak to peak voltage outputted by the third stage on the actual circuit, as well as there being a larger capacitance in the peak detector causing a slower decay of the output voltage.

5 Conclusion

In conclusion, even though the real-world circuit operates as intended and compares favourably with simulated results (indicating the possibility of a high manufacturing yield), I would not recommend it for use in the FYGER project for several reasons.

Firstly, the range of the system is low, limiting the area the robots can be used in and potentially causing health and safety issues.

Secondly, the system requires direct line of site operation between the Infrared LED and Photodiode. This is very difficult to achieve with a robot that can turn a full 360° and thus block the Infrared Wave at any time. Add the fact that the photodiode cannot detect over a very large area and the system becomes almost unusable.

Finally, the wide bandwidth of the Resonant Circuits in the real-world system means that cross talk between nearby Carrier Frequencies is very likely. This would again render the system ineffective as no team would be able to control an individual robot in a race.

I would criticise the constructed circuit of a few counts. Firstly, the 100µF capacitor had to be desoldered as it was initially placed incorrectly. Secondly, some of the solder joints have been cut back past the lead. This causes unnecessary stress on the components and can lead to damage. Finally, the circuit would look slightly neater if all the resistors were placed in the same direction.

I would suggest the following improvements for the design of the circuit. Use of higher tolerance resistors in the resonant circuits would ensure the correct Quality Factor and Bandwidth were achieved, limiting the possibility of crosstalk.

Instead of Transistors, Operational Amplifiers could be used to ensure a much more repeatable gain between circuits.

A wider receiver area for the photodiode could be used to reduce the directionality of the receiver system, making the robots easier to pilot when using this design. It would also be beneficial to have the ability to select the carrier frequency used, potentially allowing people to use frequency bands that are further apart and reduce the chance of cross talk.

Also, a unique signature could be encoded into the transmitter signal so that only a specific decoder would respond to a specific transmitter. The signature would have to be programmable to maintain the flexibility of the system.

Alternatively, low cost Bluetooth or WIFI Integrated Circuits such as the ESP8266 could be used to solve the problem. This would allow for many more robots to be controlled at the same time by completely removing issues with cross talk via the use of a protocol such as UDP.

6 References

[1] The University of Sheffield, “Individual Construction Project,” The University of Sheffield, Sheffield, 2018.

[2] P. Horowitz and W. Hill, The Art of Electronics, 3 ed., New York, NY: Cambridge University Press, 2015.

[3] Analog Devices, “LTSpice,” 9 April 2018. [Online]. Available: http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html. [Accessed 5 May 2018].

[4] P. Raybaut and G. Davar, “Python XY,” [Online]. Available: https://python-xy.github.io/.

7 Appendices

Circuit Stage 1 - Frequency Response					
Frequency (kHz)	Frequency (Hz)	Voltage In (mVrms)	Voltage Out (mVrms)	Gain (dB)	Theoretical Gain (dB)
40	40000	8.7	127	23.28568937	17.60389345
45	45000	8.7	160	25.2920146	19.75372084
50	50000	8.7	206	27.48695936	22.12320648
55	55000	8.7	272	29.90099303	24.88805436
60	60000	8.7	371	32.59709314	28.36352853
61	61000	8.7	398	33.20727639	29.19143713
62	62000	8.7	427	33.81817245	30.07894729
63	63000	8.7	459	34.44586866	31.03441723
64	64000	8.7	495	35.10171893	32.06655388
65	65000	8.7	533	35.74415913	33.18289505
66	66000	8.7	576	36.41806462	34.38594808
67	67000	8.7	620	37.05744874	35.66407546
68	68000	8.7	670	37.731111	36.97175453
69	69000	8.7	710	38.23478192	38.19425738
70	70000	8.7	760	38.82588679	39.11401155
71	71000	8.7	790	39.16215677	39.46255707
72	72000	8.7	820	39.485892	39.12332548
73	73000	8.8	834	39.53366757	38.25495918
74	74000	8.8	834	39.53366757	37.12830142
75	75000	8.8	820	39.3866236	35.94312008
76	76000	8.8	800	39.1721463	34.79936567
77	77000	8.8	760	38.7266184	33.7347876
78	78000	8.7	720	38.35626488	32.75767279
79	79000	8.7	680	37.8597932	31.86429598
80	80000	8.7	645	37.40080924	31.04682789
81	81000	8.7	610	36.91621165	30.29664658
82	82000	8.7	570	36.32711206	29.60561766
83	83000	8.7	540	35.85749014	28.96651112
84	84000	8.7	510	35.36101847	28.3730642
85	85000	8.7	480	34.8344397	27.81990986
90	90000	8.7	380	32.80528688	25.51925085
95	95000	8.7	308	30.98062928	23.75459993
100	100000	8.7	258	29.44200907	22.3319946

Table 1: First Stage Theoretical and Actual Frequency Response Results

Circuit Stage 2 - Frequency Response					
Frequency (kHz)	Frequency (Hz)	Voltage In (mV)	Voltage Out (mV)	Gain (dB)	Theoretical Gain (dB)
40	40000	35	442	22.0270845	14.79232011
45	45000	35	564	24.14422119	16.94187269
50	50000	35	733	26.42071861	19.31084762
55	55000	35	988	29.013778	22.07461467
60	60000	35	1402	32.05359939	25.547276
61	61000	35	1516	32.73262314	26.37411256
62	62000	35	1641	33.42081073	27.26022264
63	63000	35	1780	34.12703916	28.21382919
64	64000	35	1930	34.82978529	29.24343579
65	65000	35	2089	35.51740791	30.3562736
66	66000	35	2250	36.16228948	31.55439815
67	67000	35	2405	36.74094073	32.82556495
68	68000	35	2538	37.20847147	34.12366968
69	69000	35	2630	37.51775408	35.33423032
70	70000	35	2681	37.68457539	36.24253389
71	71000	35	2677	37.67160654	36.58607546
72	72000	35	2628	37.51114633	36.25171919
73	73000	35	2545	37.23239485	35.39424799
74	74000	35	2440	36.86643564	34.27886666
75	75000	35	2324	36.44336159	33.1027996
76	76000	35	2200	35.96709273	31.96578306
77	77000	35	2077	35.46736904	30.90607314
78	78000	35	1960	34.96376054	29.93249258
79	79000	35	1849	34.45737734	29.04172203
80	80000	35	1746	33.9595239	28.22621286
81	81000	35	1651	33.47358058	27.47753261
82	82000	35	1564	33.00337409	26.78767514
83	83000	35	1484	32.54731713	26.14949827
84	84000	35	1410	32.10302137	25.55680045
85	85000	35	1344	31.68662449	25.00425804
90	90000	35	1080	29.78711422	22.70545218
95	95000	35	901	28.21313493	20.94168741
100	100000	35	774	26.89345833	19.51957593

Table 2: Second Stage Theoretical and Actual Frequency Response Results