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The University of Sheffield
Electrical and Electronic Engineering

High Efficiency Switched Mode Power Supply – Design Project

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Symbol	Units	Description
P_W	W	The power loss in the Winding of the Inductor or Transformer.
P_C	W	The power loss in the Core of the Inductor or Transformer.
σ	Sm^{-1}	The conductivity of Copper. (4.56 X 10^7 at 60°C)
K_{cu}		The Packing Factor of the windings of the Magnetic Component.
A_w	m^2	The cross sectional area of the gap in the Core for the windings.
l_w	m	The mean length of one turn around the Magnetic Core.
l_e	m	The effective length of the Magnetic Core.
A_e	m^2	The effective area of the Magnetic Core.
V_e	m^3	The effective volume of the Magnetic Core.
A_l	$nH/turn^2$	The inductance per turn of the Magnetic Core.
K_v		A material constant of the Magnetic Core. (0.862)
β		A constant of the Magnetic Core. (2.608)
α		A constant of the Magnetic Core. (1.561)
B	T	The Flux Density of the Core.
B_{max}	T	The maximum Flux Density of the Core.
f	Hz	The Switching Frequency of the SMPS.
V_{DCmin}	V	The minmum Input Voltage to the SMPS.
$\hat{I}_o$	A	The peak current in the Primary Winding.
t_{on}	s	The amount of time it takes for the MOSFET to switch on.
t_{off}	S	The amount of time it takes for the MOSFET to switch off.
L	H	The inductance of the Output Inductor.
V_O	V	The Output Voltage of the SMPS.
I_O	A	The Output Current of the SMPS.
N_{min}		The minimum number of Turns on the Inductor.
V_F	V	The Forward Voltage of the Power Diode when conducting the Output Current.
$L1$	H	The inductance of the Output Inductor.
$C3$	F	The capacitance of the Output Capacitor.
ΔV_O	V	The maximum allowed ripple of the Output Voltage.
T_s	s	The period of the switching control signal.
δ		The duty cycle of the switching control signal.
J	A/mm^2	The current density of the windings of the Inductor or Transformer.
φ	Wb	The flux in the core of the Transformer or Inductor.
R_f	Ω	The value of the feedback resistor for the integrator circuit.
C_f	F	The value of the feedback capacitor for the integrator circuit.

4 Introduction

This report covers the design and construction of a High Efficiency Switched Mode Power Supply (SMPS). Switched Mode Power Supplies are very common in modern electronic devices due to their high-performance capability despite their small, low weight form factor. A well designed SMPS can produce a high-power output and still maintain efficiencies of above 90%.

The objective of this report is to design and manufacture a high efficiency SMPS with the specifications shown in **Table 4.1** [1]. In addition, the Power Supply must be designed with as high an efficiency as possible [1].

Specification	Value
Input Voltage	20 – 30VDC
Output Voltage	5VDC
Max Output Power	30W
Ripple	5% of Nominal Output Voltage
Regulation	2% from 10 – 100% Load

Table 4.1: SMPS Design Specifications

An explanation for the overall Forward Converter circuit topology will be given. The design and manufacture of key components such as the Transformer and Inductor will be discussed with all design assumptions and decisions given with explanation. Additionally, the selection of component values for the power and feedback circuits will be discussed. Finally, the SMPS will be characterised and improvements to the design will be evaluated.

5 SMPS Topology – Forward Converter

The Forward Converter circuit topology is a commonly used SMPS setup, a diagram of the standard single switch circuit can be seen in **Figure 5.1**. The circuit operates as follows [2]:

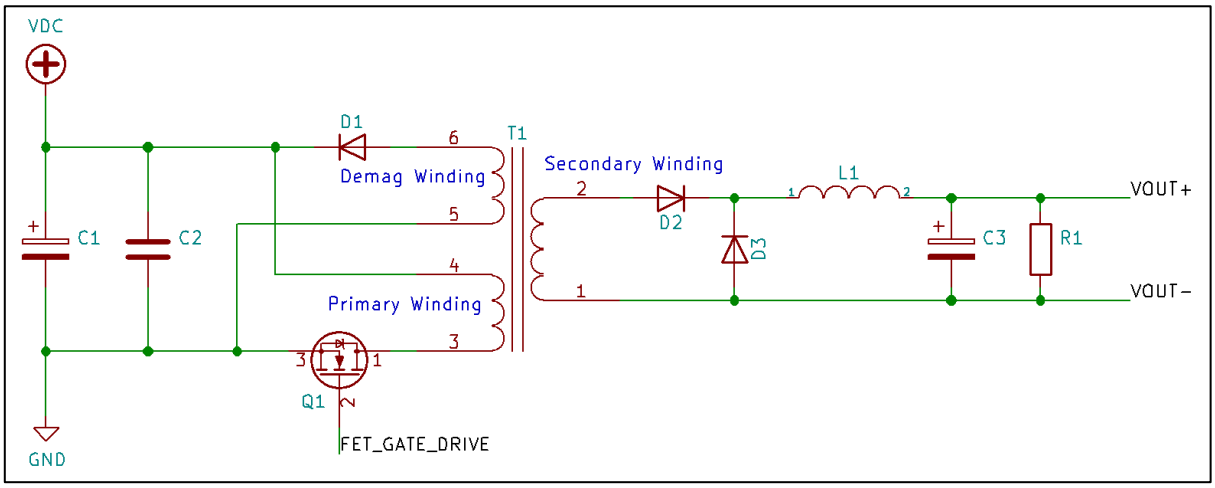

Figure 5.1: Single Switch Forward Converter Circuit Topology – Generated with KiCAD [13]

MOSFET Switched On:

1) When Q1 is switched on, the supply voltage appears across the Primary Winding. This produces a voltage across the Secondary Winding.
2) We can assume that the Secondary Winding Voltage is greater than the Output Voltage. Consequently, D2 is forward biased and current from the Secondary Winding flows through L1 into the Load (R1).

3) C3 acts to form a low pass filter configuration with L1. This smooths the current ripple on the output producing a much lower output voltage ripple.

MOSFET Switched Off:

1) When the MOSFET is switched off L1 attempts to maintain a constant current through itself, this can only occur by forward biasing D3.
2) With D3 forward biased a current loop is formed with L1, D3 and the Load. In short, L1 supplies power to the Load when the MOSFET is switched off.
3) The Demagnetisation Winding (Demag) acts to provide a current path for the Primary Winding to be demagnetised.

The use of a Forward Converter provides the following benefits to the design:

- Minimised copper losses in the Transformer as it is not being used as a Magnetic Storage element (as it is in a Flyback Converter). The output Inductor acts as the storage element [3].
- The low pass filter configuration on the output reduces ripple voltage, producing a more stable output [3].
- The Transformer allows the circuit to act in a buck or boost configuration. Additionally, it provides galvanic isolation from the supply voltage [1].

The Forward Converter topology has been selected for this project for the above reasons, despite the increased cost and size that comes with the addition of the output Inductor.

6 Initial Design Calculations

This section covers the initial design calculations and decisions that were used to select components for the Forward Converter design. These calculations provide an initial starting point for component values and provide the information required for the more complex design of the circuit's magnetic components.

6.1 Loss Estimations

The power losses within the circuit are used as a starting point for the calculation of component parameters, particularly in the initial design of the Transformer.

Initially we assume that the SMPS will be 85% efficient [1]; this efficiency can be improved with subsequent revisions to the circuit design. Additionally, we assume that the power supply will provide full load at 40% Duty Cycle to allow the Primary Winding of the Transformer time to be fully demagnetised [1]. **Table 6.1** shows the estimated power values for the SMPS.

SMPS Estimated Power Values		
Parameter	**Value**	**Units**
Output Power	30	W
Input Power	35.29411765	W
Instantaneous Power	88.23529412	W
Instantaneous Input Current	4.411764706	A
RMS Input Current	2.790244994	A
Total Power Loss	5.29411765	W

Table 6.1: Estimated Power Values for the SMPS

These estimations for power allow us to calculate the approximate power loss in each major component of the circuit based upon estimations for the percentage of the total loss each component provides. The results of these calculations can be seen in **Appendix 17.1.**

6.2 Transformer

The Transformer design revolves around the required Turns Ratio and the geometry of the selected core. 3C90 was selected as the material for the core [4], the geometry was selected from the ETD range of cores. Due to the use of the Output Inductor the Transformer requires no airgap as the Inductance of the Primary and Secondary Windings does not need to be specifically tuned [2]. As shown by **Equation 1**, we use the Power of the Transformer as a starting point as the Ampere Turns is proportional to the root of the Winding Loss [1].

$$NI = \sqrt{\frac{P_W \sigma k_{cu} A_W}{l_W}} \qquad Equation\ 1$$

Using this initial calculation and the core geometry data shown in **Table 6.2**, we can calculate the Primary Turns, Flux Density and Operating Frequency of each core [1]. The results of these calculations can be seen in **Appendix 17.2**.

Transformer Core Geometry						
Core Name	**Effective Length (mm)**	**Effective Area (mm^2)**	**Effective Volume (mm^3)**	**Winding Area (mm^2)**	**Mean Winding Length (mm)**	**A_L Value ($nH/turn^2$)**
	l_e	**A_e or A_{core}**	**V_e**	**A_w**	**l_w**	**-**
ETD29	70.4	76	5376	89	53	1950
ETD34	78.6	97.1	7640	123	60	2250
ETD39	92.2	125	11500	177	69	2470

Table 6.2: ETD Series Core Geometries for the Transformer [1]

The calculations indicate that the ETD39 core may be the best choice for efficiency. From **Equation 2** we can see that Core Loss is proportional to BF Product [1]; consequently, we want to select the core with the lowest BF Product.

$$B = \left(\frac{P_c}{V_e K_v (Bf)^{\alpha}}\right)^{\left(\frac{1}{\beta-\alpha}\right)} \qquad Equation\ 2$$

However, as we do not have calculations for Core and Winding Loss it is difficult to make a final decision on the core geometry for the Transformer. Additional calculations for the Inductor in **Section 6.4** will provide further information to aid in the selection of a core geometry.

6.3 MOSFET

As we are designing for efficiency, we wish to understand the power loss in the circuit due to the MOSFET used to perform the switching action. Calculations of the power loss in each of the available MOSFETs due to Conduction and Switching losses will help us to determine which MOSFET is most suitable for our application. The results of these calculations can be seen in **Appendix 17.3**. The characteristics of each MOSFET can be seen in **Appendix 17.4** [1].

The power loss calculations show that the best choice for efficiency is the PSMN2R7-30PL at all frequencies, due to its low On State Series Resistance. Additionally, we can see that switching loss increases with frequency, as is indicated by **Equation 3** [1]. Consequently, to optimise power loss in the MOSFET we should aim to use the lowest switching frequency possible. Unfortunately, this is in direct contrast with the power loss in the Inductor. This trade-off will be discussed further in **Section 6.4.**

$$P_{SW} = \frac{V_{DCmin}\widehat{I_1}\left(t_{on} + t_{off}\right)f}{2} \qquad Equation\ 3$$

6.4 Inductor

Correct design of the Inductor is paramount to the operation of the SMPS, too low an inductance will place the power supplies output ripple outside of specification [2]. The initial calculations for the inductor centre around **Equation 4, 5, 6 and 7** (using information from **Table 6.2**) [1].

$$L \approx \frac{5V_O}{I_O f} \qquad Equation\ 4$$

$$P_C = \frac{K_v f^{\alpha} {B_{max}}^{\beta} V_e}{10} \qquad Equation\ 5$$

$$N_{min} = \frac{I_O L}{B_{max} A_e} \qquad Equation\ 6$$

$$P_w = \frac{{N_{min}}^2 {I_O}^2 l_w}{\sigma A_w k_{cu}} \qquad Equation\ 7$$

Equation 7 shows us that the Winding Loss is primarily proportional to the number of turns, which is proportional to the switching frequency and inversely proportional to maximum flux density [1]. Additionally, **Equation 5** shows us that the Core Loss is proportional to the maximum flux density and frequency [1]. Our aim is a high efficiency SMPS; consequently, we must minimise both the Winding and Core Loss as much as possible.

A low B_{max} of 100mT was selected in order to minimise the Core Loss. **Equation 5** shows that Core Loss is proportional to B_{max}^{β}; therefore, it has a greater effect in reducing the Core Loss compared to increasing the Winding Loss. This value was based upon graphs found in the 3C90 Material Datasheet [4] and was used alongside data from **Table 6.2** to generate the results for the Inductor in **Appendix 17.5**.

The highest switching frequency of 117819Hz was selected in order to minimise the Winding Loss through reduction of the number of turns required in the Inductor. Although this selection will increase both the Switching Loss of the MOSFET and the Core Loss in the Inductor/Transformer, much greater savings are made through reducing the Winding Loss.

Finally, the largest core size (ETD39) was selected in order to minimise the Winding Loss by maximising the Winding Area of the Inductor [1]. Again, although this increases the loss in the Core the savings by reducing the Winding Loss are far greater. These decisions and assumptions were also extended to the Transformer and so the largest core size was also selected for the Transformer.

6.5 Power Diodes

Selection of the Power Diodes is based upon the Maximum Reverse Voltage they can withstand before breakdown and the average Forward Current they can conduct [1]. Of the diodes available, all three have an ample enough Reverse Voltage capability for our Output Voltage specification (5V). Additionally, the average Forward Current capability of all three diodes is more than enough for our Output Current specification (6A).

Consequently, the diodes will be selected based upon their Power Dissipation in order to maximise the efficiency of the SMPS. The Power Dissipation for each diode can be calculated using **Equation 8** [1]. The results for these calculations can be seen in **Table 6.3**.

$$P_{D2+D3} = V_F I_O \qquad Equation\ 8$$

Power Diode Power Dissipation		
Part Number	**Forward Voltage at I_O (V)**	**Total Power Loss (W)**
DSSK80-006B	0.24	1.44
8TQ100PBF	0.55	3.30
MUR840G	0.77	4.62

Table 6.3: Power Diode Power Dissipation

The information from **Table 6.3** shows that DSSK80-006B is the best choice for a high efficiency SMPS as it has by far the lowest power dissipation. Inspection of the datasheet for this diode also confirms that it can switch at our required Switching Frequency of 117819Hz [5].

6.6 Output Capacitance

The value of Output Capacitance must be selected appropriately so that the voltage ripple on the output of the SMPS is within specification (5%). Initially the minimum value of Output Capacitance can be approximated using **Equation 9** [6]. Additionally, we check this Output Capacitance value by calculating the Corner Frequency of the LC filter on the output of the SMPS using **Equation 10** [1].

$$C = \frac{V_O {T_s}^2 (1-\delta)}{8 \Delta V_O L1} \qquad Equation\ 9$$

$$f_c = \frac{1}{2\pi\sqrt{L1C3}} \qquad Equation\ 10$$

Appendix 17.6 shows the results from these calculations for all cores and available switching frequencies. These calculations indicate a required Output Capacitance of 3.05µF for the output inductance and switching frequency we have selected for our design.

6.7 Initial Design Calculations Summary

This section has allowed us to develop the initial design decisions and component selections for the SMPS. We now have selections for the MOSFET, Power Diodes and Output Capacitance, as well as some initial calculations for the circuits Magnetic Components. The selections that have been made for the circuit so far are shown in **Table 6.4**.

Initial Design Calculations Summary	
Switching Frequency	117819 Hz
Transformer and Inductor Core	ETD39
Primary Turns	24
Secondary Turns	17
Inductor and Transformer Maximum Flux Density	100mT
MOSFET	PSMN2R7-30PL
Inductor Turns	17
Required Inductance	35.4µH
Required Airgap	1.28mm
Power Diodes	DSSK80-006B
Output Capacitance	3.05µF

Table 6.4: Initial Design Calculations Summary

Additionally, we can compare the estimated power dissipation with the newly calculated power dissipation.

Power Dissipation – Estimated vs Calculated		
Component	**Estimated Power (W)**	**Calculated Power (W)**
Inductor (L1)	0.794	0.182
MOSFET (Q1)	1.059	0.69
Diode (D2)	1.324	1.44
Diode (D3)	1.324	

Table 6.5: Estimated vs Calculated Power Dissipation in Major Circuit Components

Table 6.5 shows that in total the estimated power dissipation is much higher than the calculated power dissipation. This bodes well for the efficiency of the power supply as it indicates that we may be able to reach an efficiency rating of above 85%. When we have performed our full design calculations for the Inductor and Transformer, we will have a better indication of the power dissipation in the magnetic components.

7 Magnetic Component Design

The following section covers the results of the detailed design of the SMPS's Magnetic Components (Transformer and Inductor). The correct design of the Transformer and Inductor is paramount as both components heavily influence the operation of the circuit, take a long time to produce and are difficult to modify. Optimisation of the efficiency of both components will be discussed as well as the trade-off's in cost and size that these efficiency improvements introduce. It is important to note that this section will not cover the design calculations for these components in detail, but rather focus on the design decisions made and their ramifications.

7.1 Transformer Design Calculations

The Transformer heavily influences the Output Voltage of the SMPS through its Turns Ratio, an incorrect Turns Ratio will produce an Output Voltage well outside of specification and cause issues with the SMPS's Regulation capabilities [2]. Additionally, the core of the Transformer cannot saturate as it this will introduce a non-linearity into the system and affect the SMPS's Regulation capabilities [1].

It is important to remember that we are optimising for efficiency and thus we are attempting to minimise both Core and Winding Loss. **Equations 11 and 12** show the calculation for Winding and Core Loss respectively [1], the aim of this procedure is to balance these two values in order to produce the most efficient Transformer.

$$P_W = \frac{J^2 A_W k_{cu} l_W}{\sigma} \qquad Equation\ 11$$

$$P_C = K_v f^{\alpha} \left(\frac{\varphi}{A_e}\right)^{\beta} \qquad Equation\ 12$$

As we have already fixed the size of the Transformer Core and the Switching Frequency using the initial design calculations, there are only certain parameters we can control to improve the Winding and Core Loss. **Equation 11** shows us that the Winding Loss can only be optimised by reducing the Current Density (J) or increasing the conductivity through parallel windings [1]. **Equation 12** shows us that the Core Loss can only be optimised by decreasing the Flux in the core during operation [1].

The calculations begin by resolving for the required Turns Ratio using the Duty Cycle, Output Voltage, Input Voltage and the voltage drops across the MOSFET and Power Diodes [1]. This calculation is where the behaviour of the Forward Converter, Buck or Boost, is defined. This SMPS specification requires a Turns Ratio greater than 1 as it is acting as a Step Down (Buck) converter.

A calculation for the Output Inductance is then performed as this value directly influences the current in the Primary Winding of the Transformer [1]. This initial calculation then allows for the calculation of the number of turns on the Primary Winding (and by extension the number of turns on the Secondary Winding via the Turns Ratio), the Flux Density requirement in the Core and the required conductor area for the Primary Winding [1].

Once the area for the Primary Winding conductors has been calculated the available area for the Secondary and Demagnetising Windings can be calculated [1]. For this SMPS design we are assuming that the Primary and Demagnetising Windings have a 1:1 Turns Ratio. The conductor areas allow us to calculate the actual value of Packing Factor we have achieved for the Transformer and if necessary, modify our assumptions to improve this value to be near nominal (0.5 for this SMPS) [1]. Additionally, the conductor area allows us to calculate the Current Density in the windings and verify it is within an acceptable range (2 – 5Amm^{-2}) [1].

It is important to note that these calculations are performed at the extremes of the SMPS's operation. The worst-case operating point is the minimum Input Voltage at the maximum load and the maximum Input Voltage at the minimum load. In order to compensate for these scenarios, we calculate the minimum Duty Cycle required for operation within specification assuming the maximum Duty Cycle is 40% [1].

Appendix 17.7 shows the calculated key characteristics of the Transformer based on the ET39 Core geometry; these values can now be used to construct the Transformer for use in the prototype SMPS. The actual Turns Ratio of 1.41 based upon achievable Primary and Secondary Turns counts is very close to the nominal value of 1.45, therefore no adjustment needs to be made to achieve a more accurate Turns Ratio. Additionally, the Packing Factor of 0.496 is very close to the nominal value of 0.5 [1]. Both factors indicate that this is an achievable Transformer design for real world construction by hand.

Additionally, these calculations give us a better indication of the power dissipation in the Transformer Core through the flux density. The calculated value is 44.1mT as opposed to the maximum allowed for value of 100mT; thus, Core Loss will be lower than originally anticipated leading to a more efficient SMPS.

However, as stated in **Section 6.4** the Winding Losses seem to be the main contributor to loss in the Magnetic Components. The Winding Loss can be optimised further by adding parallel windings to the Transformer design. The aim of parallel windings is to decrease the series resistance of the Transformer by using multiple conductors for the windings instead of a single, thicker conductor [7]. This not only improves the series DC resistance of the winding but also drastically improves the AC resistance by combating the skin effect [7]. Parallel Windings will be introduced in **Section 8.1** during the construction of the Transformer.

7.2 Inductor Design Calculations

As with the Transformer before, the Output Inductor heavily influences the performance of the SMPS. Too low an inductance will cause the ripple on the output of the power supply to be outside of specification [1]. Too high an inductance causes unnecessary Winding Loss due to the increased number of turns required to reach the higher inductance value [1], this is of importance given the high efficiency specification. Additionally, as with the Transformer, we must ensure that the Inductor core will not saturate during operation.

Equation 13 and **14** show the calculation for Winding and Core Loss in the Inductor respectively [1]. As with the Transformer the Core Geometry and Switching Frequency have already been fixed; therefore, the opportunity to further reduce the Core and Winding Loss is limited. **Equation 13** indicates that we can further reduce the Winding Loss using parallel windings, as with the Transformer.

$$P_W = \frac{N^2 {I_O}^2 l_w}{A_w k_{cu} \sigma} \qquad Equation\ 13$$

$$P_c = K_v f^{\alpha} \left(\frac{\Delta I B_{max}}{I}\right)^{\beta} V_e \qquad Equation\ 14$$

The approach for the calculating the required inductor parameters is based around the inductor core geometry and maximum flux density [1]. Using the value of inductance calculated in the Inductor initial design section (**Section 6.4**) the number of required turns can be calculated along with the airgap. The results from these calculations can be seen in **Appendix 17.8**.

These results were calculated using the core geometry and maximum flux density selected in **Section 6.4.** The calculated power loss in the Inductor from the initial calculations is very close to the total power loss shown here; thus, the design should be relatively efficient (approximately 85%) for a first design pass. Additionally, as with the Transformer, we will attempt to further reduce the Winding Loss using a set of parallel windings in the Inductor construction stage (**Section 8.2**).

8 Magnetic Component Construction

This section briefly covers the construction of the Transformer and Inductor and the design considerations that need to be made for real world use. A description of the construction of each component will be given as well as an analysis of their real-world characteristics (inductance, resistance, turns ratio, etc.). As we have performed all our design calculations for the circuit's magnetic components and used these values to select the circuits other components, we must construct the Inductor and Transformer accurately to achieve correct circuit performance.

8.1 Transformer Construction

The Transformer is constructed using a bifilar winding system for the Primary and Demagnetisation Windings. This aims to optimise the packing factor of the Transformer so that it's efficiency can be increased as well as ensuring close coupling between the Primary and Demagnetisation Winding [1]. The Demagnetisation Winding was wound directly around the Primary Winding in a spiral pattern. The Secondary Winding of the Transformer is placed on top of the Primary and Demagnetisation Windings; a thin layer of Kapton tape is placed between the Primary and Secondary Winding to further insulate them whilst maintaining close coupling [1].

Transformer Construction Parameters	
Parameter Name	**Value**
Primary Core Diameter (mm)	0.75
Demagnetisation Core Diameter (mm)	0.2
Primary Parallel Windings	1
Demagnetisation Parallel Windings	1
Secondary Core Diameter (mm)	0.5
Secondary Parallel Windings	4

Table 8.1: Transformer Construction Parameters

Table 8.1 shows the parameters used in the construction of the Transformer. Parallel Windings were used to decrease the resistance of the Secondary Winding; Parallel Windings were not used on the Primary Winding as this would have made routing of the Demagnetisation Winding too complex and the Primary carries a lower current, reducing loss. This decrease in resistance on the Secondary Winding will result in a lower Winding Loss in the Transformer and increase the efficiency of the SMPS.

Table 8.2 shows the characteristics of the constructed Transformer. The Turns Ratio is higher than expected, the duty cycle of the switching signal may have to be adjusted to compensate for this. The resistance of the Primary Winding is 57.6mΩ, lower than the 64mΩ predicted by design calculations. Additionally, the resistance of the Secondary Winding is 16.3mΩ, higher than the 4.5mΩ predicted by the design calculations. Overall, we can expect to see a low Winding Loss from the Transformer given these resistances. Although the Secondary Resistance is higher than the design calculations predict, the conductor sizes used are more practical in construction and have resulted in a reasonable resistance regardless of the decreased conductor diameter due to the parallel windings.

Constructed Transformer Characteristics	
Parameter Name	**Value**
Actual Turns Ratio	1.54
Primary Winding Inductance (mH)	2.14
Demagnetisation Winding Inductance (mH)	2.14
Secondary Winding Inductance (µH)	846.4
Primary Winding Resistance (mΩ)	57.6
Demagnetisation Winding Resistance (mΩ)	Unmeasurable
Secondary Winding Resistance (mΩ)	16.3

Table 8.2: Constructed Transformer Characteristics

8.2 Inductor Construction

The construction of the Inductor winding is much simpler than the Transformer as it is only comprised of one coil. The complexity in construction comes from the addition of the airgap to the magnetic core; due to the use of an ETD core design, we only need to introduce half the airgap at the sides of the core as there is also a gap in the centre [1].

Inductor Construction Parameters	
Parameter Name	**Value**
Core Diameter used (mm)	0.4
Parallel Windings	5
Airgap on each side (mm)	0.64

Table 8.3: Inductor Construction Parameters

Table 8.3 shows the construction parameters used for the Inductor. As described previously, the airgap from **Appendix 17.8** has been halved to account for the ETD core geometry. Additionally, as with the Transformer, parallel windings have been used in the construction of the winding.

Constructed Inductor Characteristics	
Parameter Name	**Value**
Series Resistance (mΩ)	20.7
Inductance (µH)	51.9

Table 8.4: Constructed Inductor Characteristics

Table 8.4 shows the characteristics of the constructed Inductor. Due to inaccuracies in the calculation of the airgap, the actual Inductance is higher than the required value**.** The required air gap to achieve this value was 2mm total (1mm on each side). This has the benefit of producing a smaller ripple on the output voltage of the SMPS but will increase losses in the Inductor core.

The parallel windings have produced a series resistance of 20.7mΩ in the winding, this is greater than the 6.4mΩ predicted by the Inductor design calculations. This is due to an error in the calculation of the necessary number of parallel windings for the conductor diameter used in order to maintain the same conductor area. Consequently, a higher Winding Loss than calculated is expected across the Inductor.

9 Initial Circuit Simulation

Using the measured characteristics of the Transformer and Inductor a LTSPICE Model of the SMPS circuit without feedback was constructed. This model allows for fine tuning of the output capacitance for low output voltage ripple.

Figure 9.1 shows the LTSPICE Model. The Transformer is substituted for two coupled Inductors with a perfect coupling ratio and the Demagnetisation Winding has been removed from the model as LTSPICE will not simulate the magnetic properties of the circuit. Additionally, the MOSFET has been replaced with a Voltage Controlled Switch along with a Pulsed Voltage Source for the MOSFET driver circuit. It is important to note that this is a model of the circuit at full load.

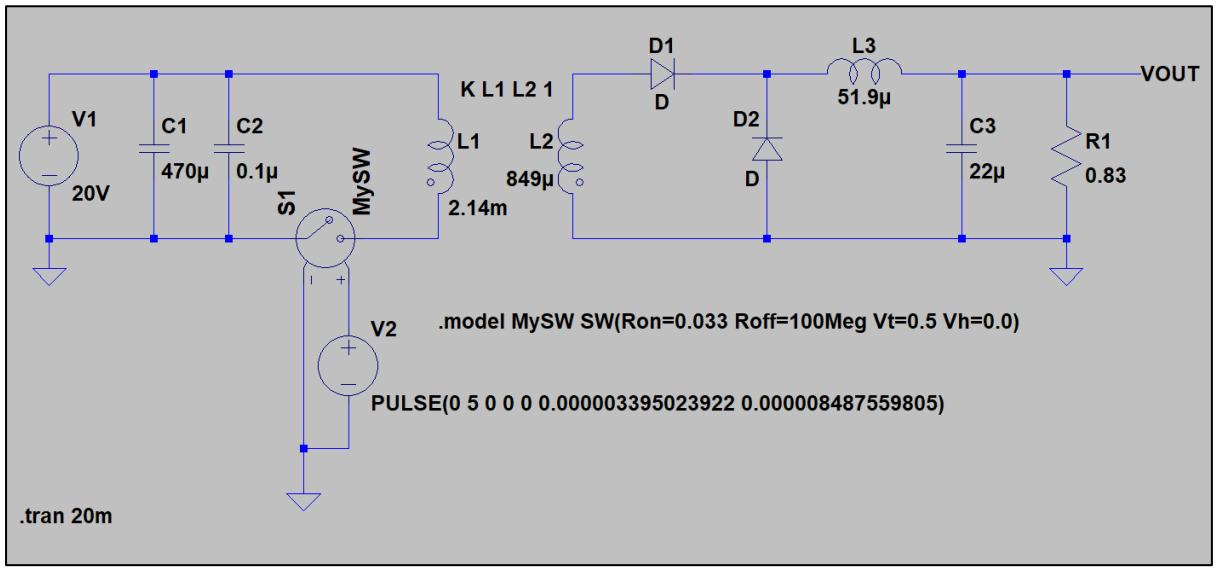

Figure 9.1: LTSPICE Model of the Forward Converter Circuit without feedback

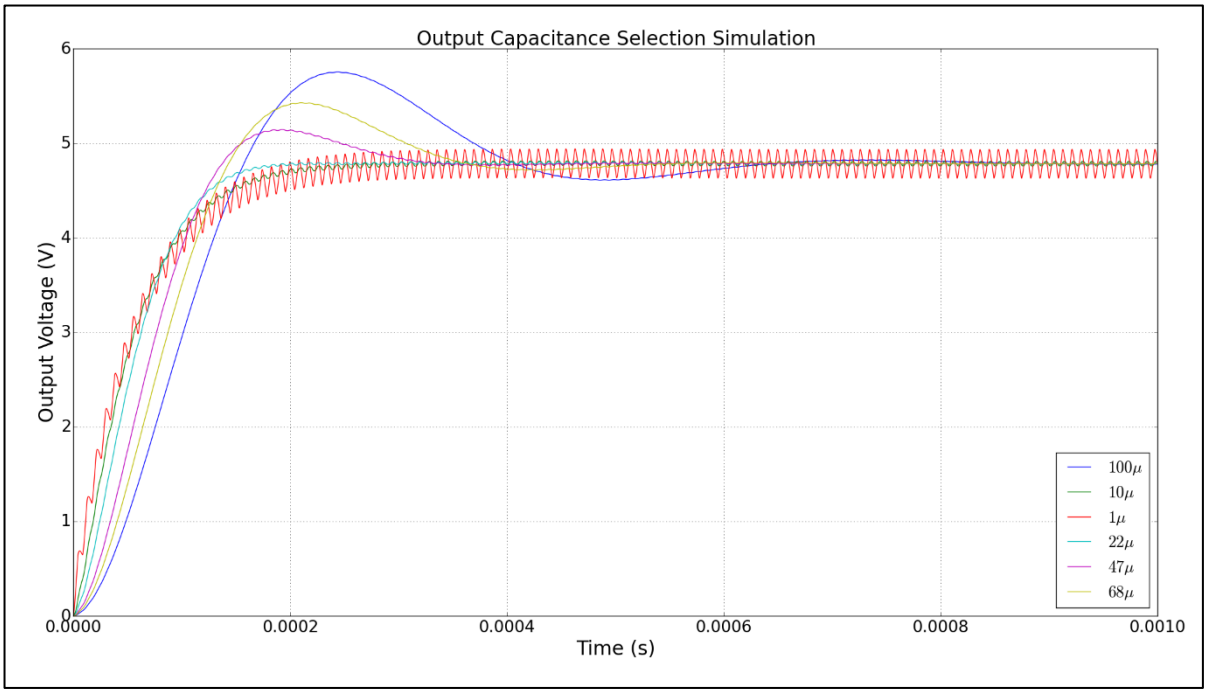

Figure 9.2: LTSpice Model simulation showing Output Voltage with varied Output Capacitance C3

Figure 9.2 shows the results from a simulation where the value of Output Capacitance was stepped through common values including and above the value of capacitance calculated in **Section 6.6.** This simulation shows that varying the Output Capacitance has a significant effect on the output ripple voltage as expected; however, it additionally affects the peak start up voltage and settle time of the output voltage. From the simulation a value of Output Capacitance of 22µF was selected as this provided the best compromise between settle time, peak start up voltage and output voltage ripple.

10 Feedback Circuit and Switching Oscillator

This section briefly covers the topology and component values used to complete the SMPS' feedback circuit used to control the Regulation. Use of the correct component values is important to ensure the power supply regulates correctly and does not oscillate.

10.1 Feedback Circuit Topology

An integrator was selected for the feedback circuit as this allows for zero error in the output of the power supply assuming it is in steady state at 5V. This integrator is formed using the Operational Amplifier integrated into the SG3524 control IC alongside a feedback resistor and capacitor. The output voltage of the SMPS is fed into the Operational Amplifier through a potential divider which can be tuned using a potentiometer. The reference voltage for the integrator is set at 2.5V.

10.2 Feedback Circuit Component Values

The value of the feedback resistance in the potential divider is set so that when the Output Voltage is 5V the potential divider will output 2.5V and match the reference voltage. A value of 15KΩ was selected. This resistance comprised of a fixed value of 10KΩ and a potentiometer of 10KΩ with the wiper connected to the output of the potential divider and set to half way. To complete the potential divider another fixed 10KΩ resistor was placed between the other leg of the potentiometer and ground.

To ensure the SMPS remains stable at its operating frequency a value of K for the integrator frequency response must be calculated so that at -30° phase (the phase that allows for a 60° phase margin on the circuits oscillation point) the feedback gain of the circuit is 0dB [1]. The value of K is found from the Bode Plot in **Figure 10.1**, as the frequency at which the 20dB per decade frequency response of the integrator crosses the 0dB point.

Using the feedback resistance, value of K and **Equation 15** the value of the feedback capacitance was calculated to be 36nF. In the construction of the circuit the closest available value of 33nF was used.

$$K = \frac{1}{R_f C_f} \qquad Equation\ 15$$

10.3 Switching Frequency Oscillator Component Values

The values of R_T and C_T must be calculated in order to tune the frequency of the switching oscillator to the chosen switching frequency (117819Hz). As per the manufacture datasheet, the switching frequency is calculated using **Equation 16** [8, p. 14].

$$f \approx \frac{1.30}{R_T C_T} \qquad Equation\ 16$$

A value of 1nF for C_T was chosen, giving a value of 6.02KΩ for R_T. A 10KΩ potentiometer was used in the construction of the actual circuit to provide tuning functionality for the switching frequency.

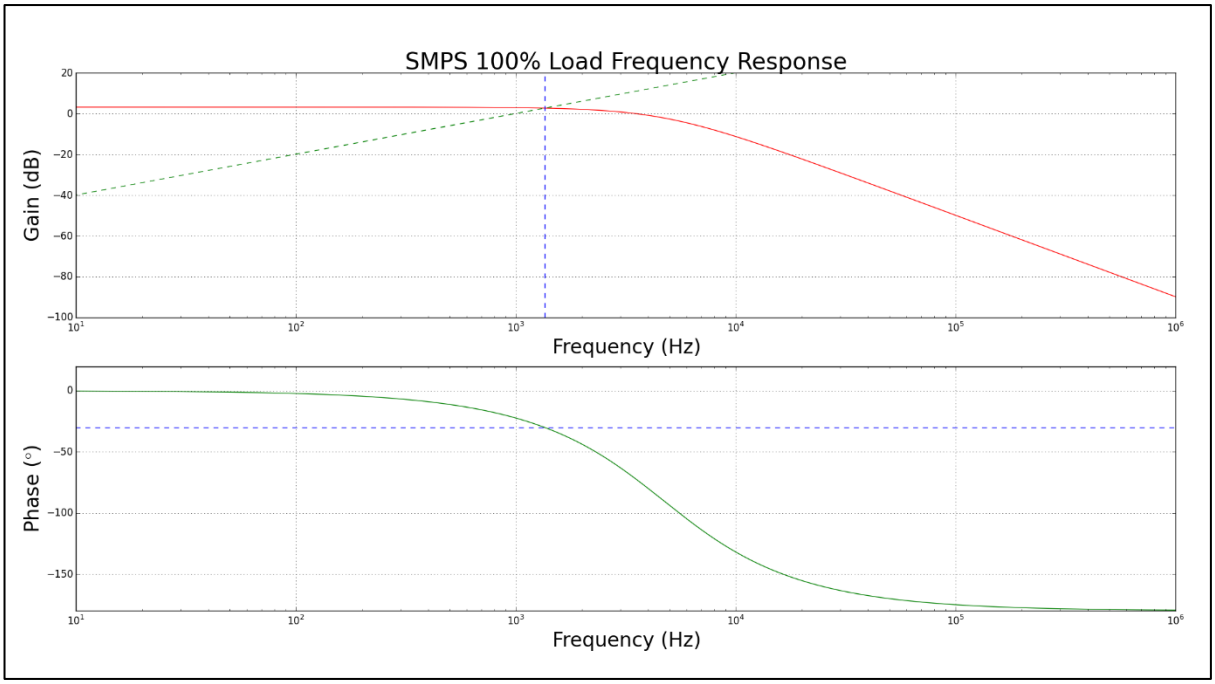

Figure 10.1: K Value calculation from uncompensated SMPS Frequency Response Bode Plot

11 Thermal Solution

Due to the high efficiency requirement of the power supply design, the largest available heatsinks paired with Mica and Thermal Paste were used to keep the MOSFET and Power Diode cool. Excess heating could cause additional losses in both components, reducing efficiency.

12 Initial Testing

This section covers the results and findings from the initial testing of the SMPS after construction using the component values detailed in the previous sections of the report. The aim of this testing is to produce a set of design revisions to improve the power supplies performance in the key areas of the specification; ripple, regulation and efficiency.

12.1 Regulation and Efficiency Testing

Regulation and Efficiency Testing were completed at this stage and raised several issues and improvements to the design that could not be completed due to time constraints. These items will be discussed in the discussion section of this report. The results for Regulation and Efficiency from this initial testing stage can be seen in **Appendix 17.9** and **Appendix 17.10**.

12.2 Ripple Testing

The output ripple of the SMPS was measured using a Keysight 2000 Series Oscilloscope [9] and the manual cursors function to ensure the high frequency peaks in the signal were not included in the measurement. The ripple was tested at both 20 and 30V Input Voltages across the full load range of the power supplies specification (10 – 100%).

Figure 12.1 and **Figure 12.2** show the results from the output ripple test. The peak ripple on the output voltage measures approximately 19%, well outside of the specification value of 5%. It is therefore clear that LC filter on the output of the power supply is not filtering the switching frequency correctly.

Consequently, the Output Capacitance value must be increased to reduce the ripple voltage on the output of the supply. By extension, this will also trigger a change in the Feedback Capacitance.

12.3 MOSFET Over Voltage

Later inspection of the PSMN2R7-30PL MOSFET datasheet indicates that it cannot operate at 30V. Consequently, a change to a MOSFET that can operate across the full Input Voltage range is required.

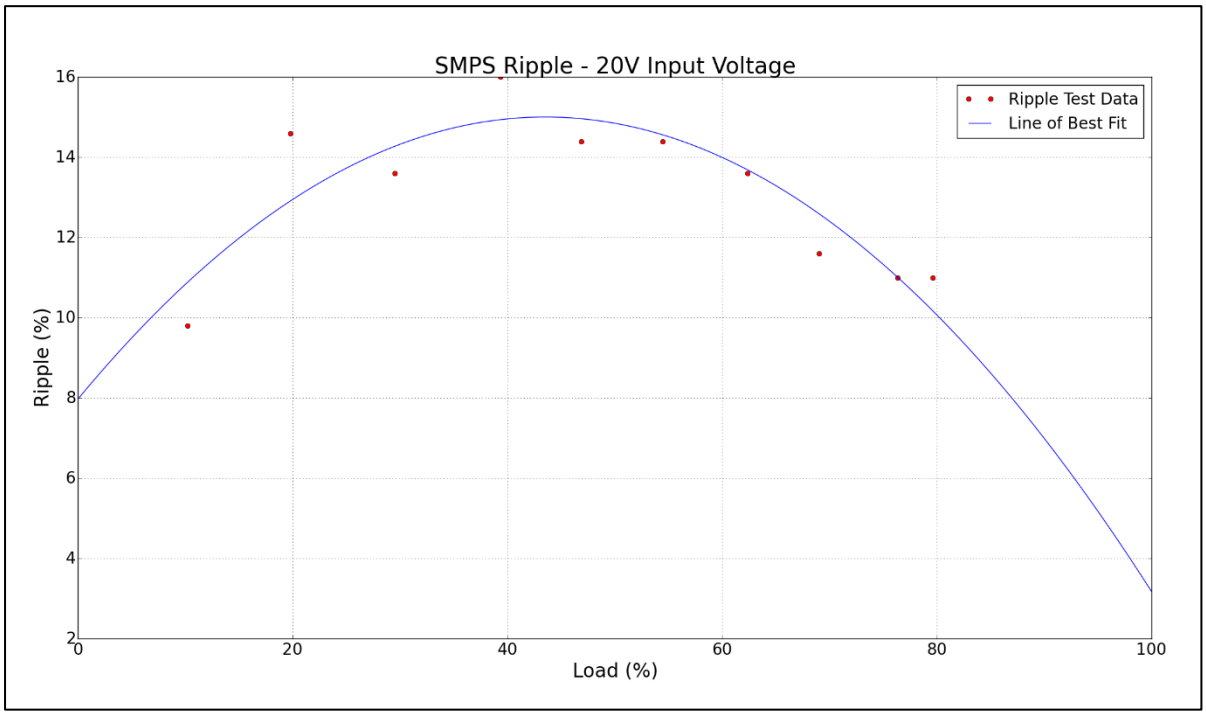

Figure 12.1: Initial SMPS Testing Output Ripple - 20V Input Voltage

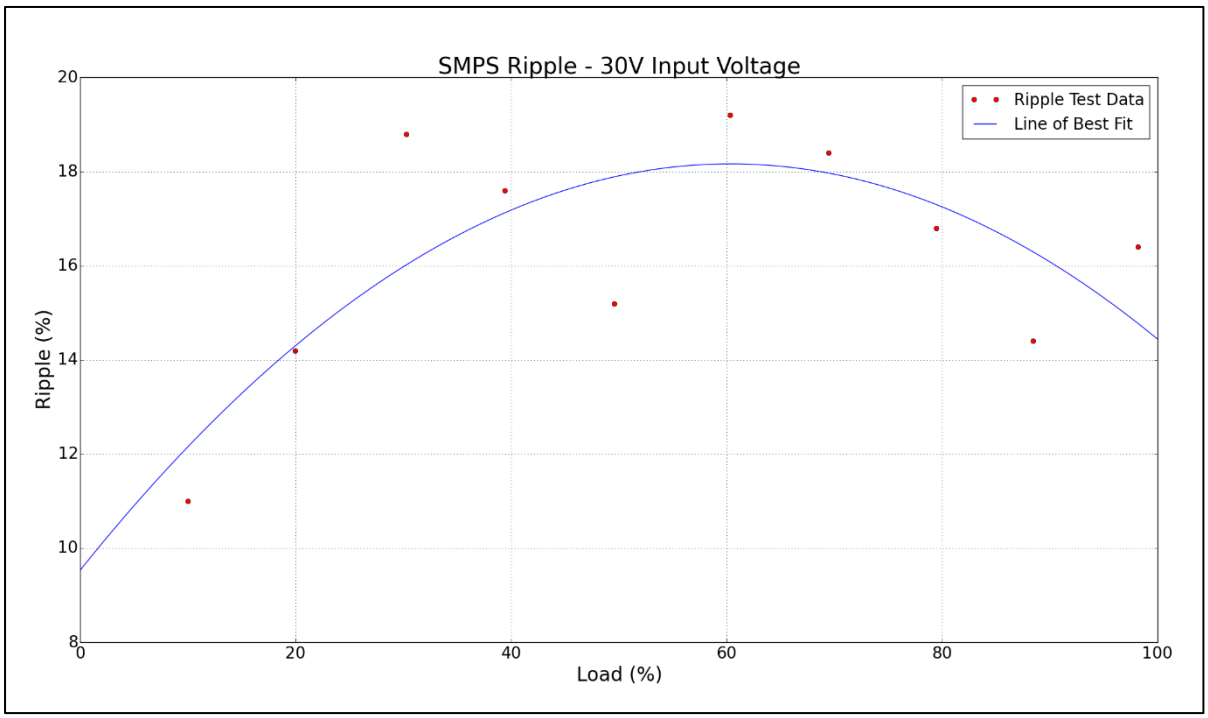

Figure 12.2: Initial SMPS Testing Output Ripple - 30V Input Voltage

13 Design Changes

This section covers the design changes completed as a result of the initial testing of the SMPS. These changes primarily aim to solve the issues with the output ripple and MOSFET that were found, but also aim to improve the overall efficiency.

13.1 Output Capacitance

Through a series of trial and error tests where the output capacitance was increased through steps of 68µF, 100µF, 220µF, 470µF and 680µF; a final output capacitance value of 470µF was found. This value was deemed to decrease the ripple to an acceptable level without being too high a capacitance value that the component was overly large or expensive. A small 1nF capacitor was also introduced in parallel to remove some of the high frequency ringing present in the output voltage.

13.2 Feedback Capacitance

To ensure that the feedback circuit still operates correctly and to prevent the introduction of any oscillations into the output of the power supply the feedback capacitance must be changed to accommodate the new LC filter on the output. After recalculations across the range of Output Capacitances that were tested, an optimal value of 150nF was found.

13.3 MOSFET

As the PSMN2R7-30PL could not operate at 30V (as this is its rated breakdown voltage) it had to be replaced with the next most efficient MOSFET capable of operating across the full Input Voltage range. Inspection of **Appendix 17.3** shows that the next most efficient MOSFET is the STP40NF10 [10]. Furthermore, inspection of the device datasheet indicates that it can comfortably operate at 30V and 4A and thus it is suitable for our application.

14 Final Testing and Discussion

This section details the procedures and results from the final suite of testing completed to characterise the Switch Mode Power Supply. Again; Efficiency, Regulation and Output Ripple will be tested and compared to the specification from **Section 4**.

14.1 Regulation

Regulation testing aims to characterise the power supplies ability to maintain a stable output voltage at varying loads. The test was performed for both 20 and 30V Input Voltages across the full load range of the power supply. A bench Multimeter [11] was used to measure the output voltage alongside a handheld unit to measure the output current. Input current and voltage were taken from the bench DC power supply [12] readout. The duty cycle of the MOSFET was measured using an oscilloscope [9] connected to the MOSFET gate. A Rheostat was used between resistances of 8.3Ω and 0.83Ω to vary the load on the supply.

Figure 14.1 and **Figure 14.2** show the results for 20 and 30V Input Voltages respectively. The results at 20V clearly indicate that the power supply fails to regulate across the full load range and only successfully regulates up to 30% load. At 40% load the duty cycle of the switching circuit tops out at 40%, as designed. At 30V Input Voltage the power supply successfully regulates within the 2% regulation specification across the full load range.

A quick solution to this Regulation performance may be found through tuning the reference voltage for the feedback circuit to offset the duty cycle range. However, for this large a discrepancy it is likely the Transformer requires reconstruction, or the design calculations need to be tweaked. Ultimately, the problem stems from the Turns Ratio of the Transformer. **Appendix 17.7** quotes a required Turns Ratio of 1.41, whereas the constructed Transformer has a ratio of 1.54 (**Section 8.1**). As the Turns Ratio is too high, the resultant Secondary Voltage will be too low to generate a stable 5V output across the full load/input voltage range. To solve this problem, the number of turns on the Secondary Winding needs to be increased to reduce the Turns Ratio.

14.2 Efficiency

Efficiency testing aims to characterise the power loss across the circuit required to produce the stable output voltage. This test is important as the specification demands a focus on efficiency. The same setup as the Regulation test was used across the full load range at 20 and 30V Input Voltage.

Figure 14.3 and **Figure 14.4** show the results for 20 and 30V Input Voltages respectively. It is important to note that due to the regulation issues the results at above 30% load for the 20V Input Voltage graph must be discounted. Regardless, the graphs show a peak efficiency of approximately 88% at 20V Input Voltage and an average efficiency of approximately 81% at 30V Input Voltage; this average efficiency is lower than the targeted 85% from the initial design calculations. As expected, an approximately quadratic curve of efficiency is shown with a peak where the switching losses and losses due to ripple balance.

Improvements to the Efficiency of the power supply can be made through a few factors. Firstly, the number of parallel windings on both the Transformer and Inductor could be drastically increased to reduce the Winding Loss by decreasing their Series Resistance. This suggestion explains the lower than expected efficiency at 30V as the parallel windings for the Inductor were miscalculated; 25 parallel windings should have been used instead of 5. Secondly, the number of turns on the Inductor could be reduced to reach the nominal Inductance value calculated in **Section 6.4**. This would reduce the Series Resistance of the Inductor but would cause an increase in ripple; thus, a corresponding increase in output capacitance would be required. Finally, the switching frequency could be increased into the megahertz to further reduce the Winding Loss; however, this would require a complete redesign.

14.3 Output Ripple

Output Ripple Testing aims to characterise the variation of the output voltage across a single switching cycle. Ideally this value should be as small as possible to ensure the power supply does not interfere with the electronics it is driving. Again, the same setup was used as in the Regulation test, however the Oscilloscope [9] was setup to measure the ripple voltage on the output of the supply using manual cursors.

Figure 14.5 and **Figure 14.6** show the results of the testing for 20 and 30V Input Voltage respectively. At both voltages the ripple is well within the specification of 5%, with both being less than 1% across the full load range. This indicates that the increase in output capacitance has sufficiently solved the ripple problem. As expected, the ripple increases at the higher input voltage of 30V due to the lower duty cycle used to maintain the same output voltage. Further revisions to the output capacitance would only need to be made if other major design changes were considered. For reference, a capture of the circuits output ripple from the oscilloscope can be seen in **Appendix 17.14.**

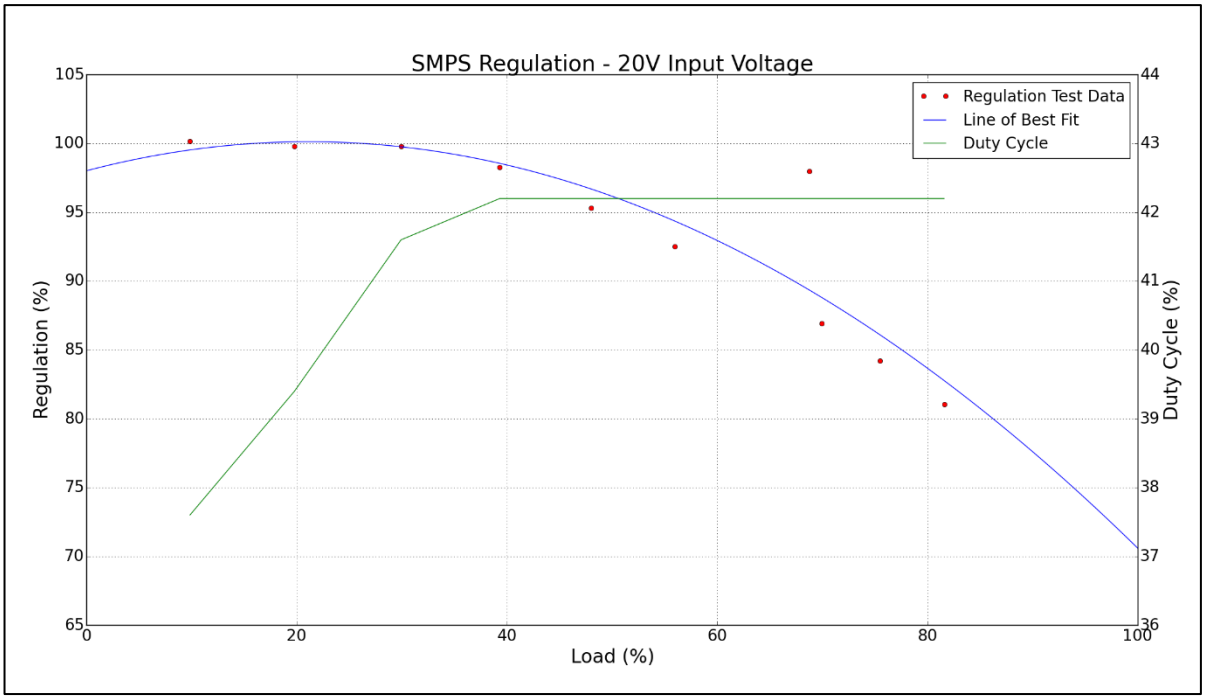

Figure 14.1: Final SMPS Regulation Testing - 20V Input Voltage

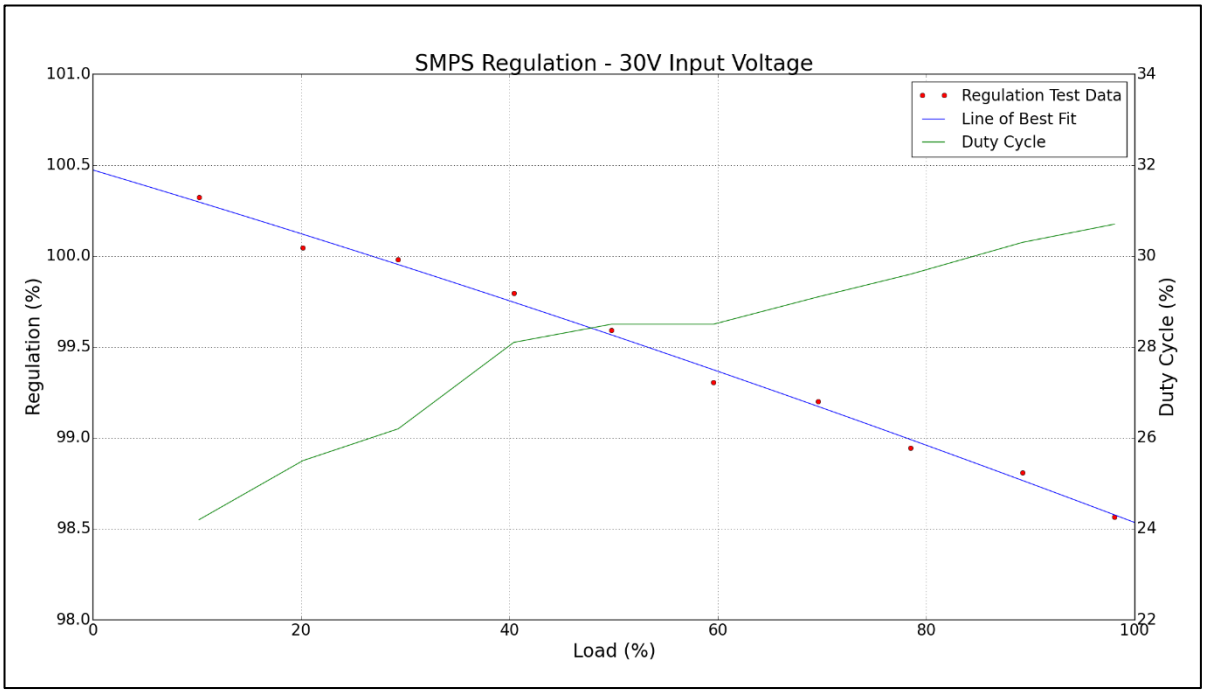

Figure 14.2: Final SMPS Regulation Testing - 30V Input Voltage

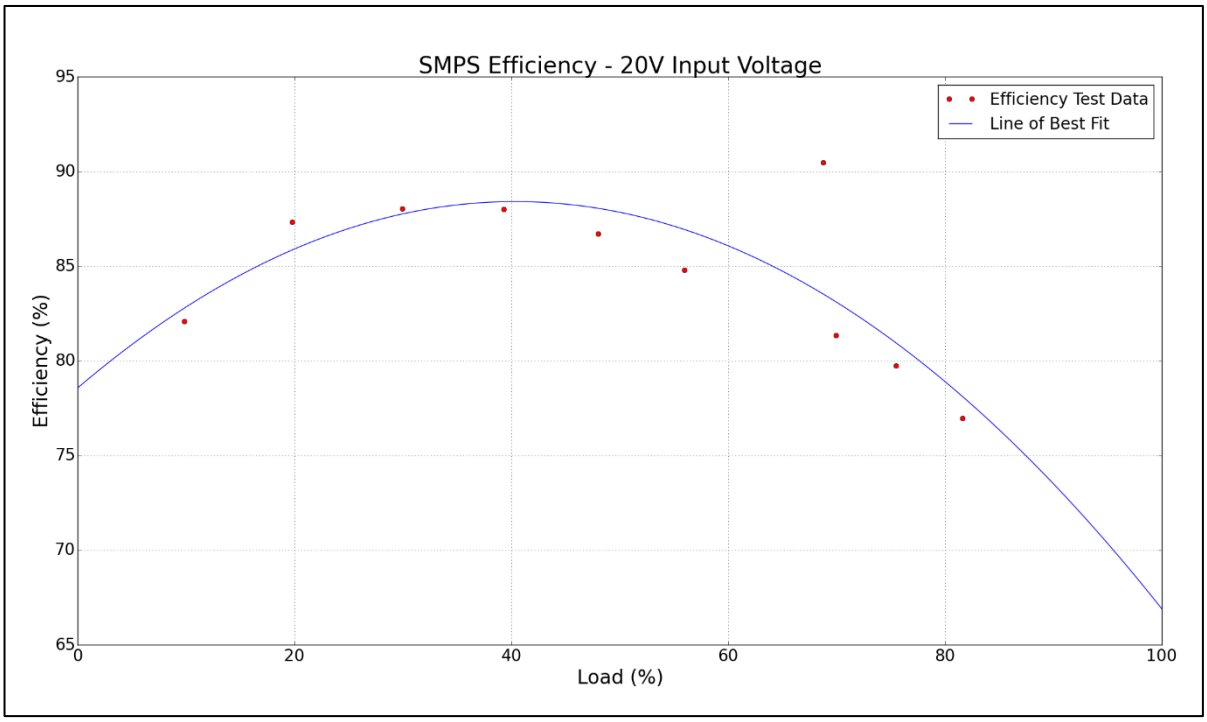

Figure 14.3: Final SMPS Efficiency Testing - 20V Input Voltage

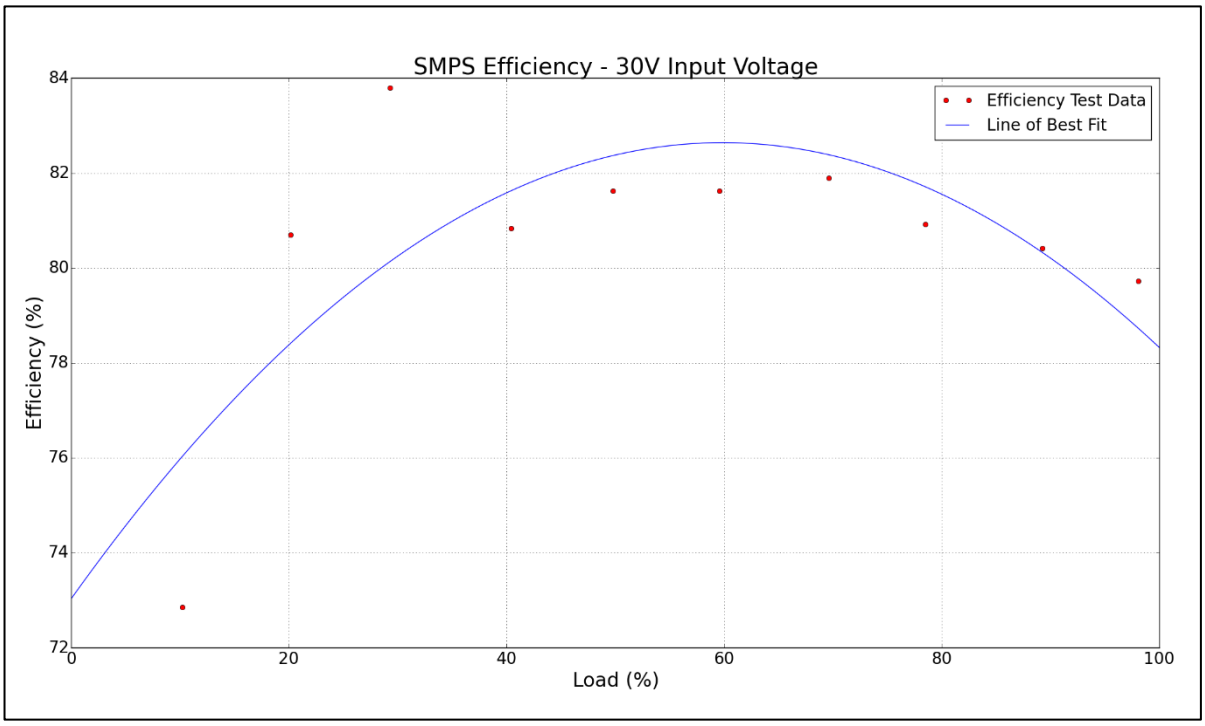

Figure 14.4: Final SMPS Efficiency Testing - 30V Input Voltage

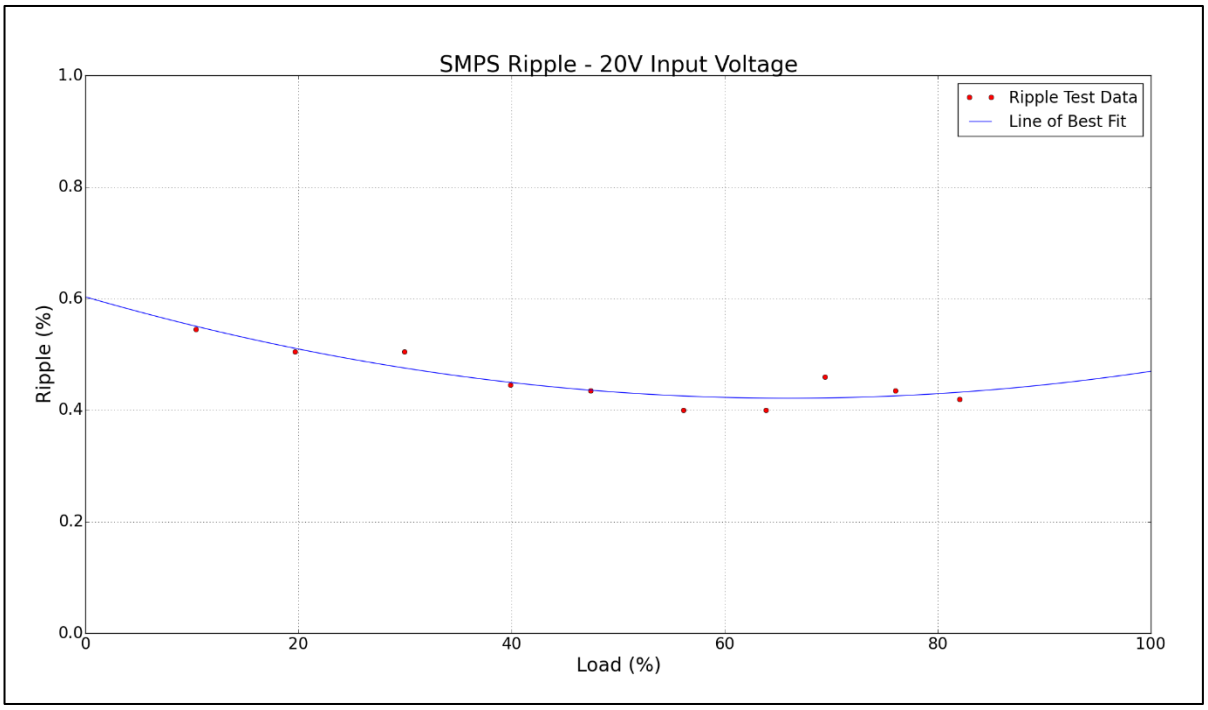

Figure 14.5: Final SMPS Ripple Testing - 20V Input Voltage

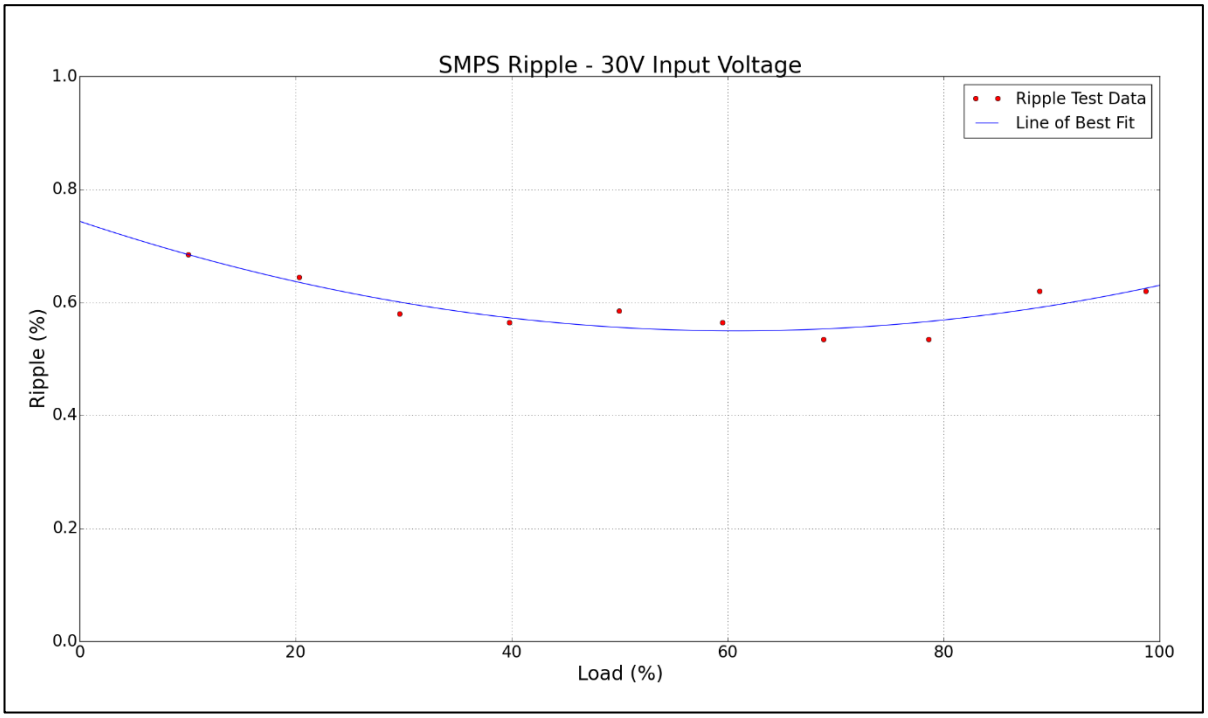

Figure 14.6: Final SMPS Ripple Testing - 30V Input Voltage

15 Conclusion

To conclude, we must evaluate the performance of the constructed Switched Mode Power Supply against the initial specification from **Section 4**. This evaluation can be seen in **Table 15.1.**

Parameter	Specification	Met?	Actual
Input Voltage	20-30V	No	Approx 25-30V
Regulation	2% from 10 – 100% Load	Partial	Met across range of 25-30V Input Voltage
Ripple	5%	Yes	-
Efficiency	85% (Initial)	Partial	Average 81%, Peak 88%

Table 15.1: SMPS Specification vs Actual Performance

The information in **Table 15.1** shows that the SMPS can operate correctly at 30V at a lower than expected efficiency. It is expected that with further design revisions this topology and general component selection (Transformer/Inductor Core Size, etc.) will produce an efficient SMPS. These conclusions are backed up by the data collated in the Appendix and the information presented in **Section 14**.

The Regulation issues will be resolved by reducing the Transformer Turns Ratio by increasing the number of turns on the Secondary Winding. The efficiency of the SMPS could be improved using the following recommendations. Firstly, increase the number of parallel windings used in both the Transformer and Inductor to reduce the series resistance of the windings and improve Winding Loss. Secondly, reduce the number of turns on the Inductor to reach the calculated Inductance and increase the output capacitance accordingly to maintain output ripple performance. Thirdly, increase the overall switching frequency of the unit to further reduce the Winding Loss from the Inductor and Transformer. Finally, attempt to find a MOSFET that will perform at the required power rating with a much lower power dissipation. For reference, the completed SMPS is shown in **Figure 15.1**

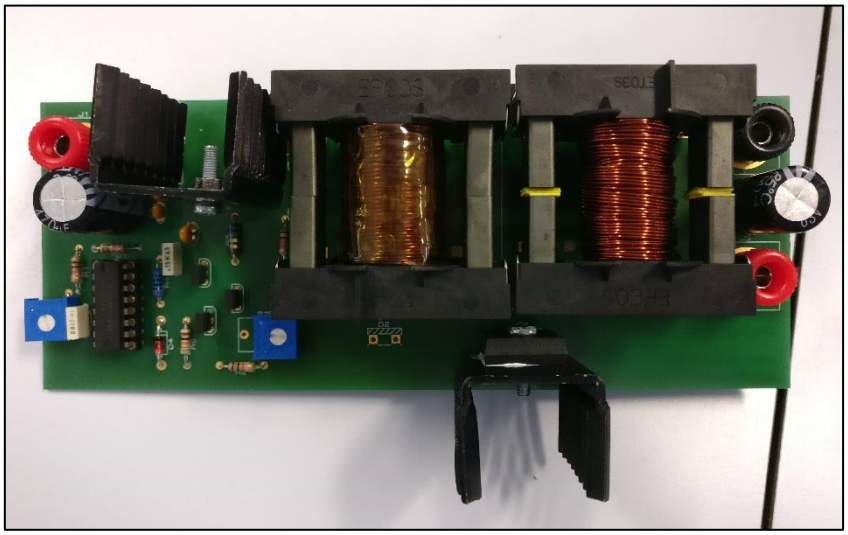

Figure 15.1: The constructed SMPS

16 References

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[14] P. Raybaut and G. Davar, “Python XY,” [Online]. Available: https://python-xy.github.io/.

17 Appendices

17.1 Estimated Major Component Losses

SMPS Estimated Major Component Losses		
Component	**Percentage of Total Loss (%)**	**Loss (W)**
Transformer Winding (T1)	5.5	0.291
Transformer Core (T1)	4.5	0.238
Inductor (L1)	15	0.794
MOSFET (Q1)	20	1.059
Diode (D1)	5	0.265
Diode (D2)	25	1.324
Diode (D3)	25	1.324

17.2 Transformer Initial Calculations

Transformer Initial Calculations					
Core Name	**Ampere Turns**	**Primary Turns**	**BF Product (THz)**	**Flux Density (T)**	**Operating Frequency (Hz)**
ETD29	105.585	18.9	6954.343	0.059	117819
ETD34	116.660	20.9	4926.411	0.071	69830
ETD39	130.499	23.4	3421.013	0.082	41608

17.3 MOSFET Power Loss Calculations

MOSFET Power Loss Calculations				
MOSFET	**Frequency (Hz)**	**Conduction Loss (W)**	**Switching Loss (W)**	**Total Loss (W)**
IRFZ24N	117819	1.09	0.32	1.41
	69830	1.09	0.19	1.28
	41608	1.09	0.11	1.20
STP40NF10	117819	0.51	0.55	1.06
	69830	0.51	0.33	0.84
	41608	0.51	0.19	0.71
IRF520	117819	3.11	0.24	3.35
	69830	3.11	0.14	3.26
	41608	3.11	0.08	3.20
PSMN2R7-30PL	117819	0.08	0.61	0.69
	69830	0.08	0.36	0.44
	41608	0.08	0.21	0.29

17.4 MOSFET Characteristics

MOSFET Characteristics				
MOSFET	**$R_{ds(on)}$ (Ω)**	**t_{on} (ns)**	**t_{off} (ns)**	**$T_{j(max)}$ (°C)**
IRFZ24N	0.070	34	27	175
STP40NF10	0.033	82	24	175
IRF520	0.200	23	23	175
PSMN2R7-30PL	0.005	82	35	175

17.5 Inductor Initial Design Calculations

Inductor Initial Design Calculations								
Core	**Frequency (Hz)**	**Required Inductance (µH)**	**Minimum Core Turns**	**Core Power Loss (mW)**	**Winding Power Loss (W)**	**Total Loss (W)**	**Current Density (Amm^{-2})**	**Core Air Gap (mm)**
ETD29	117819	35.4	27.9	2.32	0.73	0.735	3.76	2.11
	69830	59.7	47.1	1.03	2.09	2.088	6.35	3.55
	41608	100.0	79.1	0.46	5.88	5.878	10.66	5.96
ETD34	117819	35.4	23.3	3.30	0.42	0.422	2.27	1.76
	69830	59.7	39.3	1.46	1.19	1.194	3.84	2.97
	41608	100.0	66.0	0.65	3.36	3.359	6.44	4.98
ETD39	117819	35.4	17.0	4.97	0.18	0.182	1.15	1.28
	69830	59.7	28.6	2.20	0.50	0.507	1.94	2.16
	41608	100.0	48.1	0.98	1.42	1.423	3.26	3.62

17.6 Output Capacitance Calculations

Output Capacitance Calculations			
Inductance (µH)	**Switching Frequency (Hz)**	**Capacitance (µF)**	**Corner Frequency (Hz)**
35.40	117819	3.05	15311
	69830	8.69	9074
	41608	24.50	5407
59.70	117819	1.81	15311
	69830	5.15	9074
	41608	14.50	5407
100.00	117819	1.08	15311
	69830	3.08	9074
	41608	8.66	5407

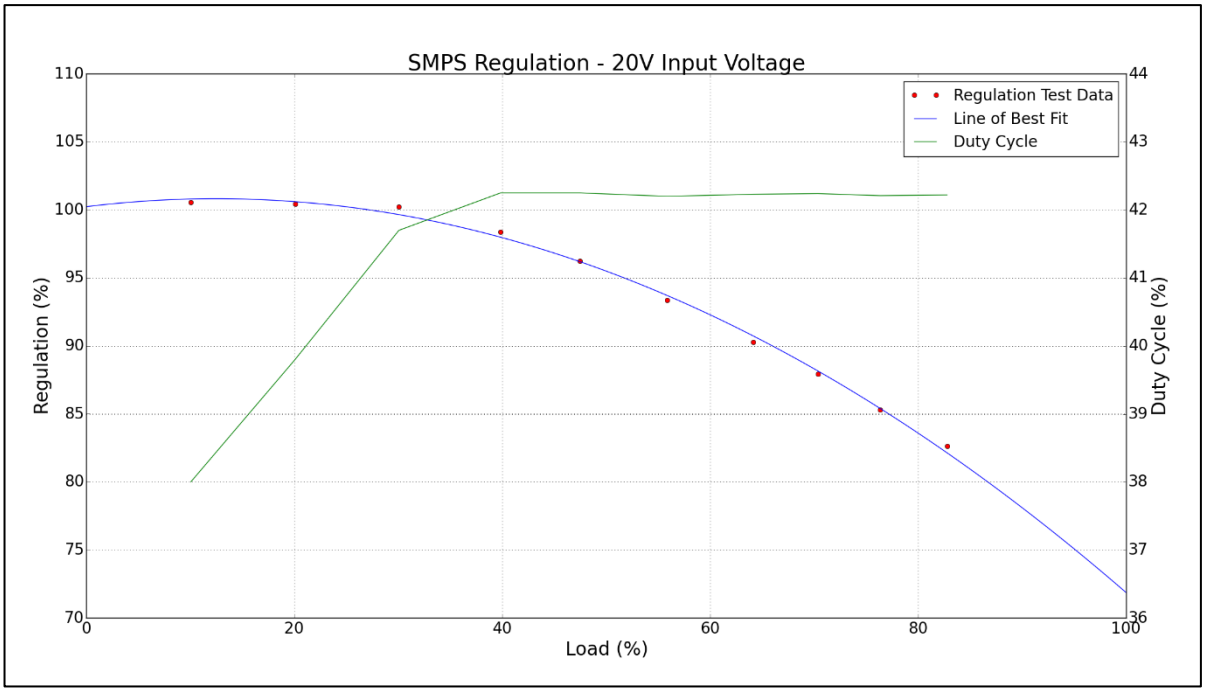
17.7 Transformer Key Characteristics

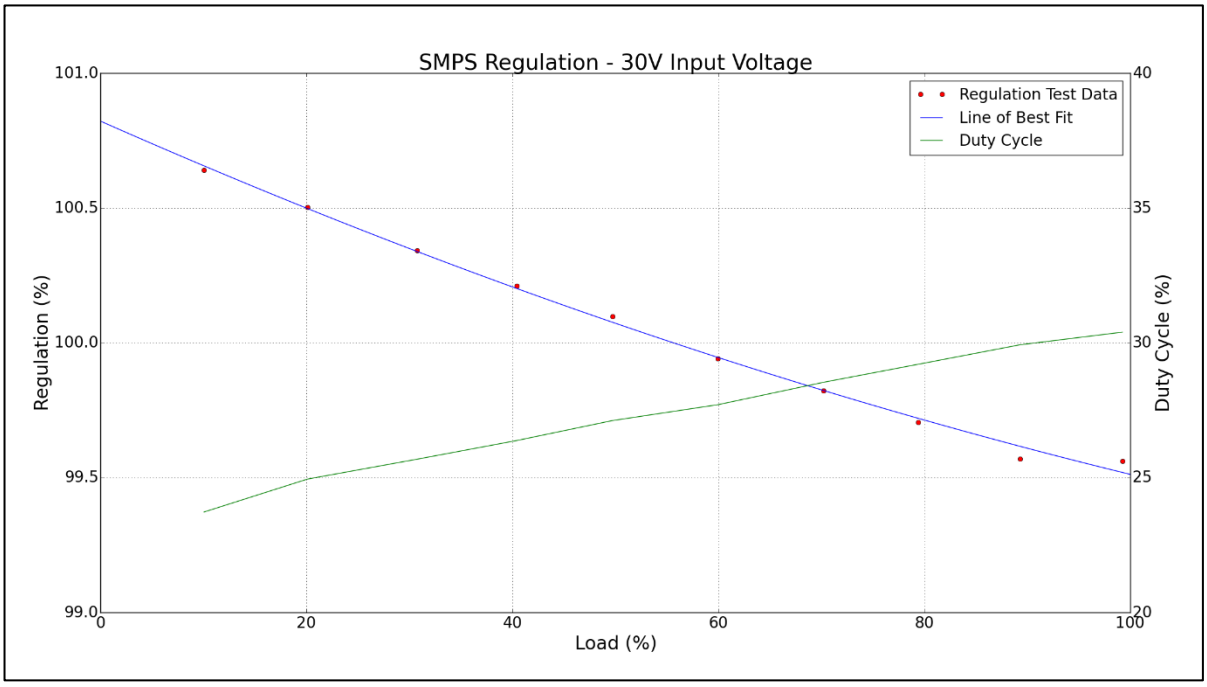
Transformer Key Characteristics	
Transformer Parameter	**Calculated Value**
Turns:	
Turns Ratio	1.45
Primary Turns	24
Secondary Turns	17
Actual Turns Ratio	1.41
Conductors:	
Primary Conductor Area (mm^2)	1.83
Actual Primary Conductor Area (mm^2)	0.442
Demagnetisation Conductor Area (mm^2)	0.031
Secondary Conductor Area (mm^2)	4.66
Primary Conductor Diameter (mm)	0.76
Nearest Primary Conductor Diameter (mm)	0.75
Demagnetisation Conductor Diameter (mm)	0.2
Secondary Conductor Diameter (mm)	2.4
Actual Packing Factor	0.496
Duty Cycle:	
Minimum Duty Cycle (%)	19
Flux:	
Flux Density (mT)	44.1
Transformer Currents:	
Peak Magnetising Current (mA)	36.4
True RMS Primary Current (A)	3.161

17.8 Inductor Key Characteristics

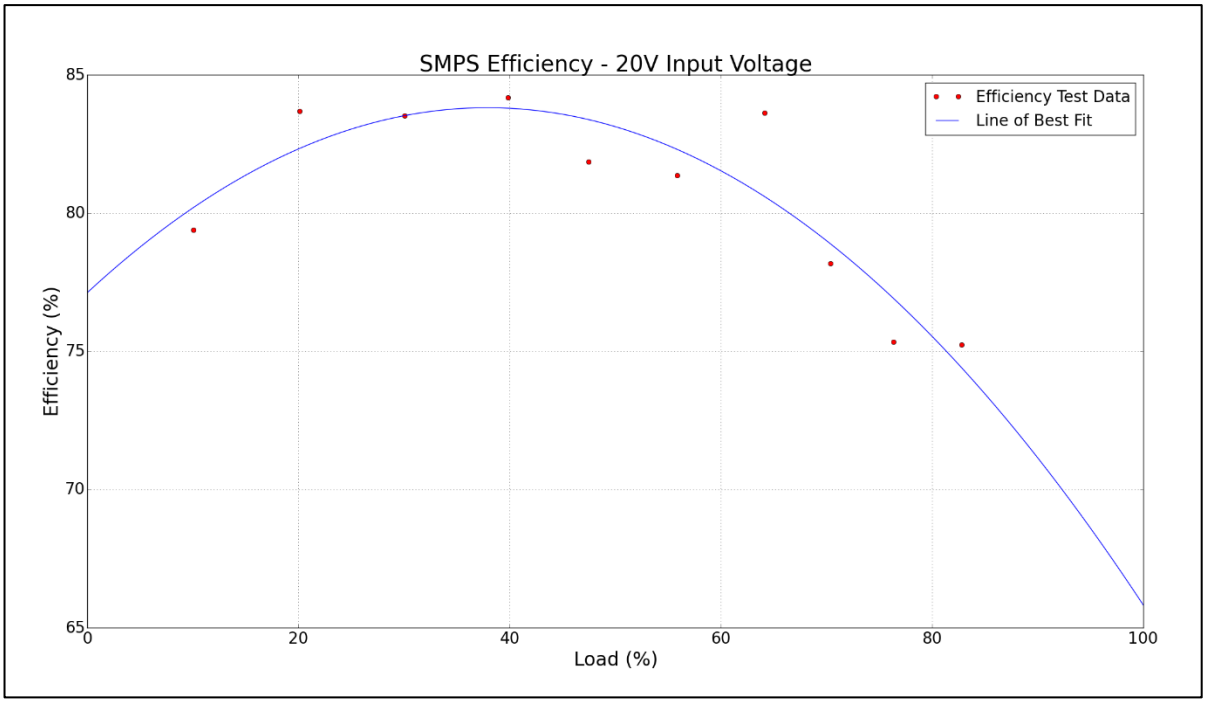
Inductor Key Characteristics	
Inductor Parameter	**Value**
Inductance (µH)	35.4
Maximum Flux Density (mT)	100
Core Air Gap (mm)	1.28
Minimum Turns	17
Core Loss (mW)	0.82
Winding Loss (W)	0.18
Conductor Diameter (mm)	2

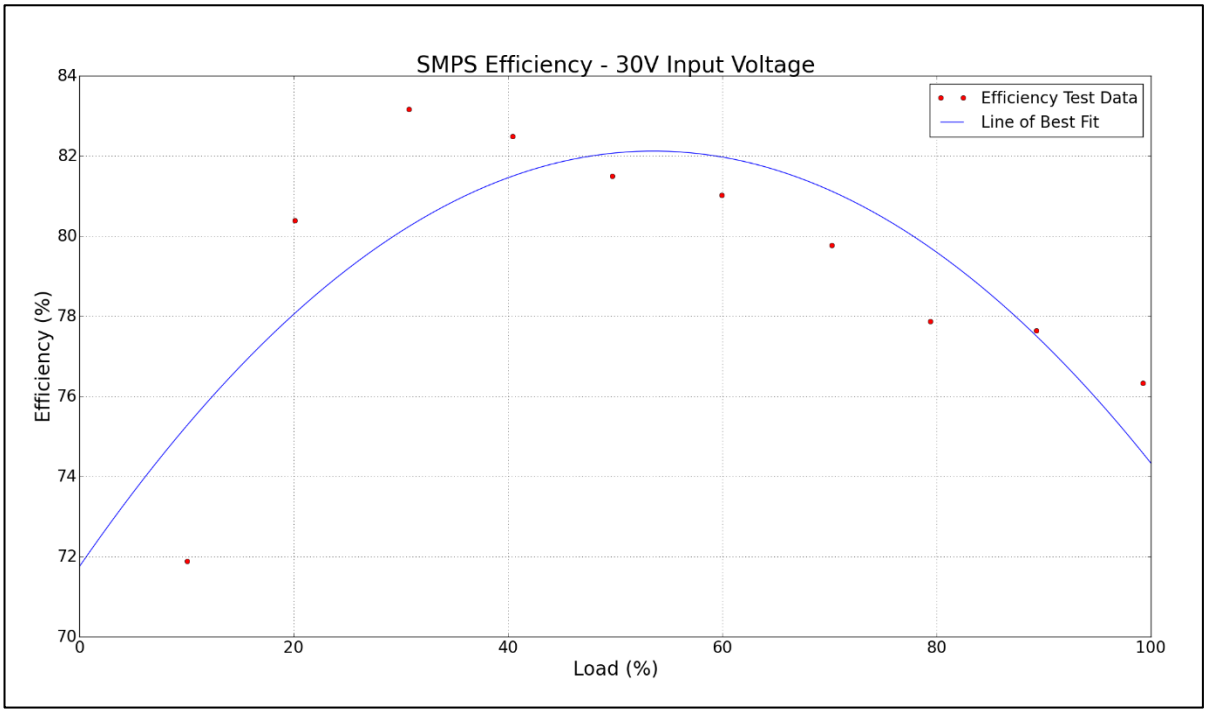
17.9 Initial Regulation Testing Results



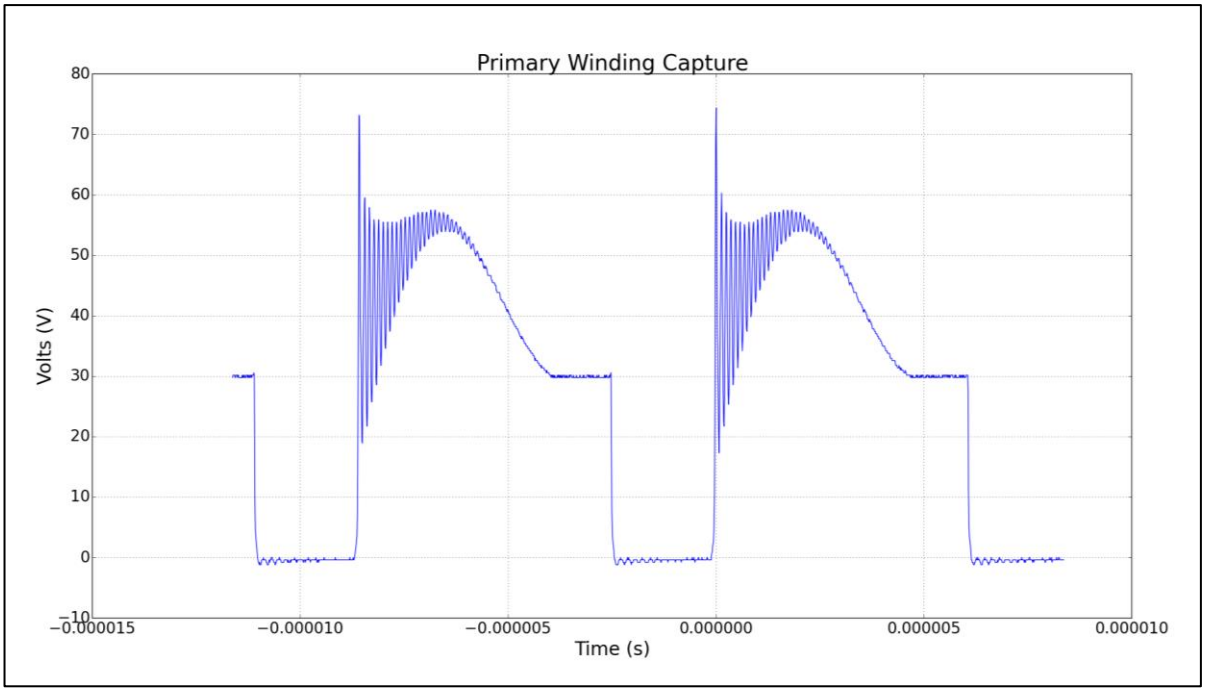


17.10 Initial Efficiency Testing Results

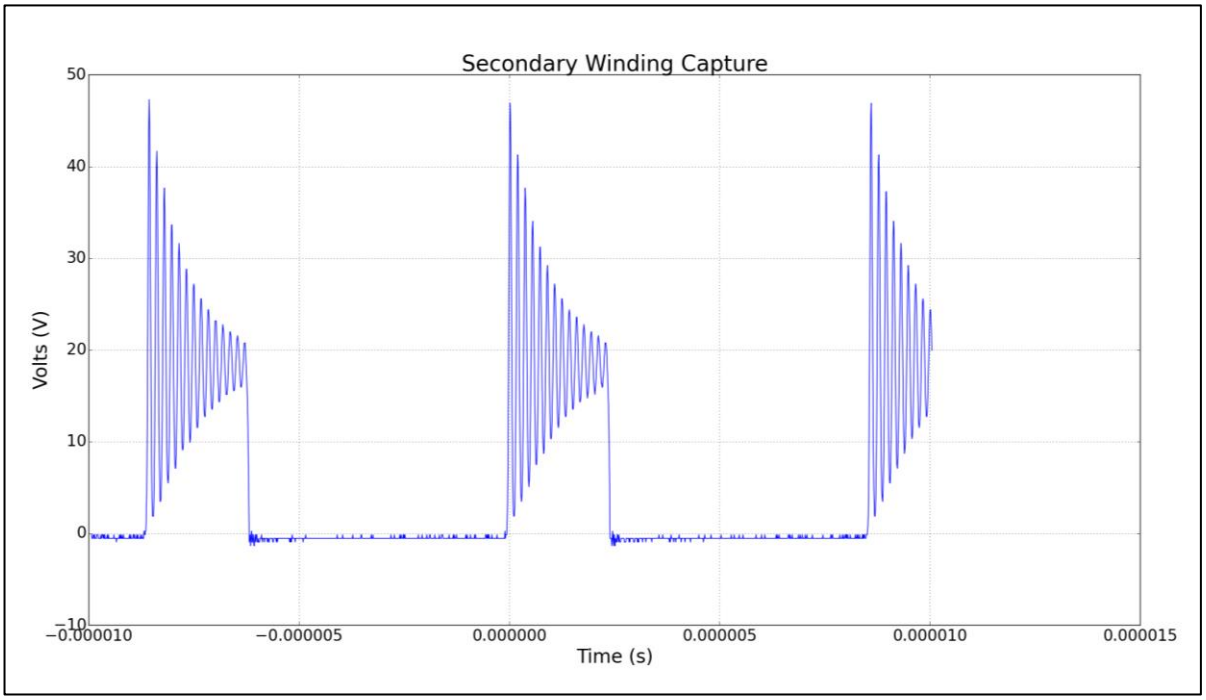




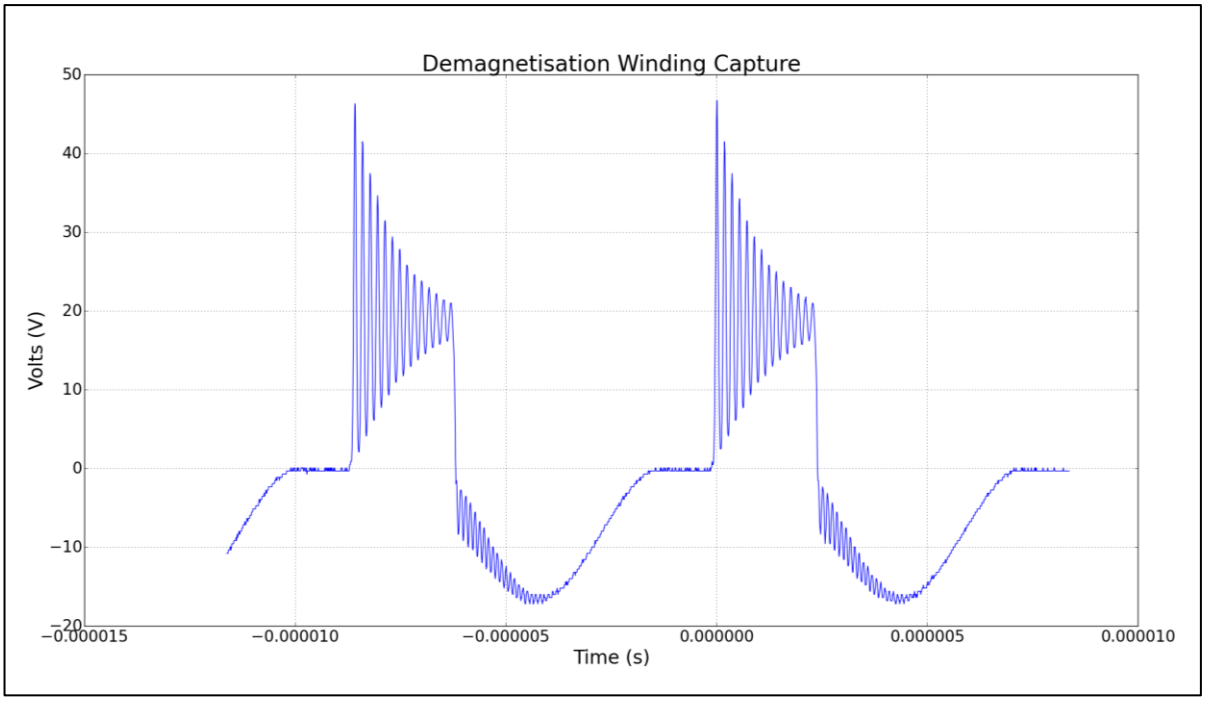
17.11 Primary Winding Oscilloscope Capture during operation



17.12 Secondary Winding Oscilloscope Capture during operation



17.13 Demagnetisation Winding Oscilloscope Capture during operation



17.14 Output Voltage Ripple Capture during operation