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The University of Sheffield
Electrical and Electronic Engineering

Schottky Diode – Lab Report

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1 Contents

2 Introduction

This report aims to outline the work completed for the Schottky Diode Laboratory in the Diamond Clean Room. The process of fabricating and characterising a Schottky Diode will be covered along with sample data from the devices produced during the Laboratory. This sample data will be analysed to indicate the success of the device fabrication and any improvements that could be made.

Schottky Diodes are very commonly used in high speed switching applications due to their low turn on voltage allowing for fast switching cycles [1]. They are typically found in communications and switching power supply applications and thus are extremely prevalent throughout modern electronic devices where efficiency is of paramount importance [1]. Every modern Smart Phone contains a Schottky Diode.

Schottky Diodes are formed by Metal Semiconductor Junctions [1] [2]. This junction is the root cause of the low turn on voltage of the devices [1] [2]. The physics surrounding the Schottky Diode and Ohmic Metal Semiconductor junctions will also be discussed in this report.

3 Metal Semiconductor Junction Theory

3.1 Rectifying Metal Semiconductor Junctions (Schottky Diode)

A rectifying contact is formed between a metal and an n-type semiconductor when the work function of the metal is greater than that of the semiconductor [1] [2].

When the metal and the n-type semiconductor are joined the fermi levels equalise. Free electrons in the semiconductor flow into the metal, as it has a lower work function [1] [2]. This generates a depletion region of positively charged donor atoms on the semiconductor side. No depletion region exists on the metal side due to the excess of available negatively charged electrons [2]. This has the effect of bending the conduction and valence energy bands upwards in the depletion region [1] [2].

Via thermionic emission small amounts of electrons can move from the metal to the semiconductor [1] [2]. Small amounts of electrons also have enough energy to cross the potential barrier and flow from the semiconductor to the metal [1] [2]. When the junction is in equilibrium (no bias voltage applied) these currents are equal [1] [2]. An energy band diagram of the junction in equilibrium can be seen in **Figure 2**.

When the metal is biased positively with respect to the semiconductor (forward biased) the fermi level and energy bands of the semiconductor move upwards and the potential barrier is reduced [1] [2]. This allows a greater flow of electrons from the semiconductor to the metal. The flow of electrons from the metal to the semiconductor remains the same [1] [2]. Behaviour of the junction in the forward biased region can be described by **Equation 1**.

$$J = J_0 \left[e^{\left(\frac{qV}{nk_BT}\right)} - 1 \right] \tag{1}$$

Where J_0 = Reverse Saturation Current Density, q = 1.6x10^{-19} (Electron Charge), V = Junction Bias Voltage, n = Non-Ideal Diode Factor, k_B = 1.38x10^{-23} (Boltzmann Constant), T = Temperature in °K.

When the metal is biased negatively with respect to the semiconductor (reverse bias) the fermi level and energy bands of the semiconductor move downwards and the potential barrier is increased [1] [2]. This further restricts the flow of electrons from the semiconductor to the metal. A small current is produced by electrons flowing from the metal to the semiconductor via thermionic emission [1] [2]. The current density behaviour of the junction in the reverse biased region can be described by **Equation 2**.

$$J = -J_0 \tag{2}$$

Measurements of the change in junction capacitance with respect to voltage can be used to calculate the donor density of the semiconductor using **Equation 3**.

$$N_d = \frac{2}{A^2 q \varepsilon_0 \varepsilon_r} \times \frac{dV}{dC^{-2}} \tag{3}$$

Where A = Cross Sectional Area, ε_0 = 8.8x10^{-12} (Permittivity of Free Space), ε_r = Relative Permittivity, C = Capacitance. The donor density and capacitance can then be used to calculate the Junction Barrier Voltage using **Equation 4**.

$$C = A \left(\frac{q \varepsilon_0 \varepsilon_r N_d}{2(V_{Barrier} + V_{bias}} \right)^{\frac{1}{2}} \tag{4}$$

Using a modified version of **Equation 1** with n = 1, T = 300°K and I_0 = 1nA a typical Schottky Diode IV Characteristic can be generated. This typical characteristic can be seen in **Figure 1**.

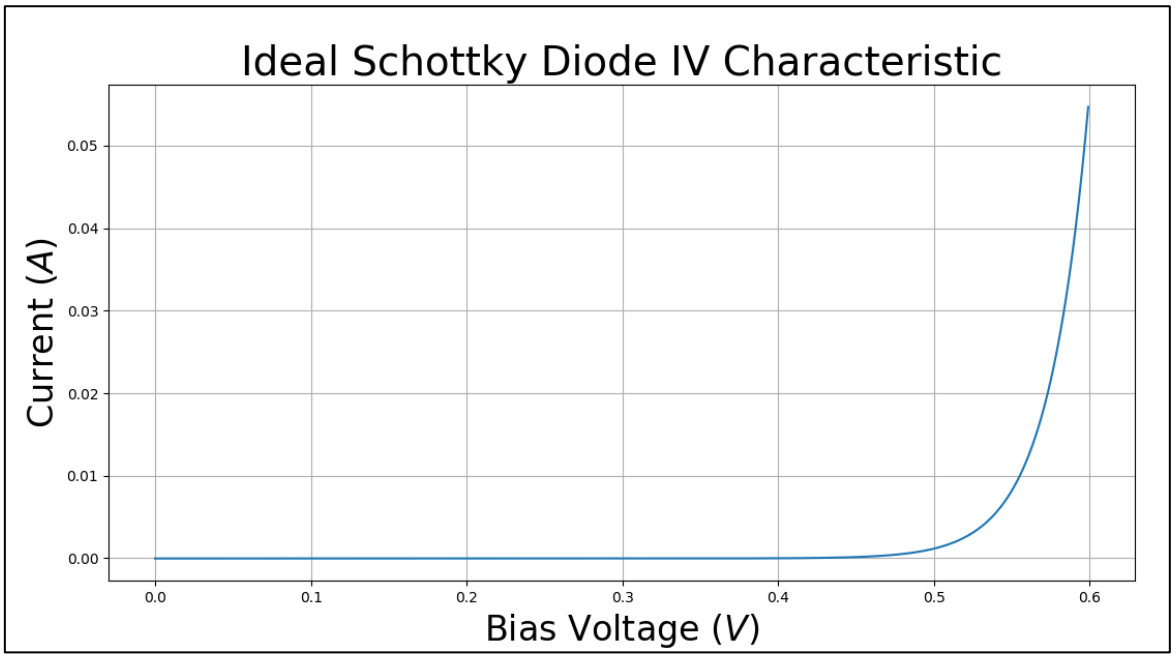

Figure 1: Ideal Schottky Diode IV Characteristic

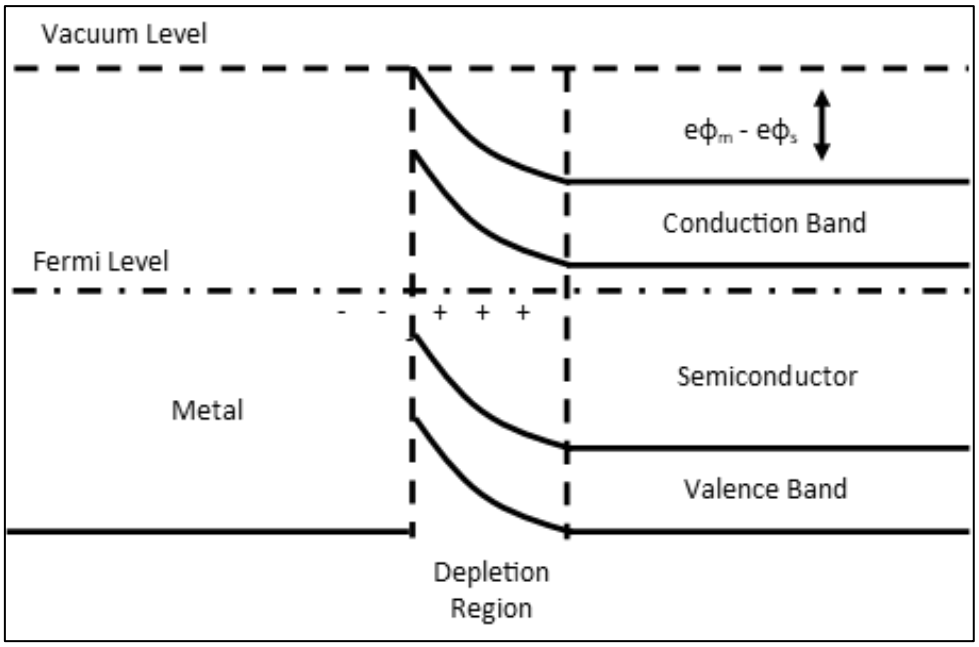

Figure 2: Metal Semiconductor Junction Equilibrium Energy Band Diagram

3.2 Ohmic Metal Semiconductor Junctions

An ohmic contact is formed between a metal and an n-type semiconductor when the work function of the semiconductor is greater than that of the metal [1] [2].

When the semiconductor and the metal are joined the fermi levels equalise via electrons flowing from metal to semiconductor. No depletion region is formed on the side of the metal or the semiconductor, thus there is no potential barrier for free electrons to cross [1] [2]. Consequently, it is easy for current to flow in either direction across the junction, regardless of the bias [1] [2].

Due to surface states generated at the semiconductor metal junction by distorted bonds in the semiconductor, the above description does not hold [1]. The surface states in the semiconductor generate a fixed potential across the junction, regardless of the metal used [1]. This makes it very difficult for current to flow in either direction. This is caused by the electronic levels the surface states generate, which tend to lie in the band gap [1].

Instead, we use quantum tunnelling effects to produce the ohmic contact. Instead of surmounting the potential barrier, we send electrons through it [1] [2]. We attempt to make the width of the depletion region caused by the potential barrier as low as possible by doping the semiconductor very heavily [1] [2]. This makes it very easy for the electrons to tunnel through the barrier as they need a much lower energy to do so [1] [2].

4 Device Fabrication

4.1 Safety

Before entering the clean room, all required Personal Protection Equipment must be worn. This includes shoe covers, goggles, a smock and a hair net. When working with chemicals nitrile gloves must be worn. All chemical work must be completed in a laminar flow cabinet. Before working with a chemical, consult its Safety Datasheet [3] [4].

When working with DC and AC Supplies the standard operating procedures must be followed. Care must be taken to only activate the supplies when necessary and to not touch live circuitry. Electrical testing should not be performed in the same area as chemical processes [3] [4].

Schottky Diode production involves the use of hot plates. Use tweezers to pick up devices on the hot plate and always switching off the hot plate when finished to avoid burns [3] [4].

When operating the probe stations take care to move the probes out of the way when placing a device on the station. The probes are very sharp and may stab you [3] [4].

4.2 Clean Room Specification

The fabrication of semiconductor devices is severely affected by small solid particles in the air. To minimise the presence of these particles, a clean room is constructed where the air is continuously filtered and circulated [3].

To do this, clean rooms are built to an “ISO” standard or class, which specifies the level of purity in the air and the environmental conditions [3]. The main diamond clean room is Class 7, the yellow room (used for photolithography) is Class 6 [3]. The lower the class number the purer the air [3].

Ideally the flow of air within a clean room should be laminar [3]. Laminar flow cabinets achieve total laminar flow, the rest of the clean room does not [3].

4.3 Cleaving, Cleaning and Mounting

Before fabrication can occur, the wafer must be broken down into dimensions just large enough for the device [5]. Semiconductor wafers are extremely expensive (5cm diameter Gallium Arsenide Wafer approximately £100), thus we attempt to use as little of the wafer as possible to fabricate our device. The wafers are split using a diamond tipped scriber [5].

Following cleaving, the sample is cleaned using N-butyl acetate heated to 100°C for 1 minute [5]. A cotton bud is dipped in N-butyl acetate before being rotated across the surface of the sample, this is performed on filter paper [5]. The sample is placed in N-butyl acetate heated to 100°C for another minute before being washed in acetone and isopropyl-alcohol. It is dried using a stream of nitrogen [5]. The acetone removes any debris from the cotton bud; isopropyl alcohol ensures no streaks are left on the surface of the sample which could affect later optical processes [5].

Finally, the sample is mounted on a silicon carrier making it easier to handle in later processes. This is completed using wax.

4.4 Photolithography Process

The photolithography section of fabrication is when the semiconductor wafer is etched away to leave the structure of the desired devices.

The sample is dried on a hot plate at 100°C for 1 minute to remove any water it has absorbed. The sample is then placed in a spinning machine and held in place by a vacuum; it is spun for 30 seconds at 3000rpm with a constant stream of nitrogen applied to remove any debris [5].

Two drops of AZ 1514H Photoresist are placed on the top of the sample. It is then spun at 30 seconds at 3000rpm to spread the Photoresist evenly across the surface, forming a layer only a few micrometres thick [5]. The sample is placed on a hot plate at 100°C for 1 minute to soft bake the Photoresist, allowing it to be weakened by the UV light when it is exposed under the mask [5].

The sample is then placed under a mask and exposed to UV light for 5.3 seconds, this weakens the photoresist ready for the developer [5]. The sample is submerged in agitated AZ developer for 1 minute [5]. Finally, the sample is washed in deionised water for 1 minute and then dried using a stream of nitrogen [5].

At this stage, the sample should be verified under a Microscope for impurities and defects caused by under exposed photoresist [5].

4.5 Metallisation Process

Metallisation is the process used to deposit a metal contact on the top of the newly formed device. An evaporative metallisation process is used to form the contacts [5].

The samples are placed on a platform below a piece of tungsten filament containing 99.9% pure Aluminium; this platform is surrounded by a Bell Jar [5]. The Bell Jar is evacuated to $6x10^{-9}$ atmospheres of pressure; the Aluminium is then melted by a current passing through it, causing it to evaporate [5]. The evaporated Aluminium that hits the sample condenses, forming a thin film on the top of the device [5].

This process is performed in evacuated conditions to avoid impurities in the metal layer and to ensure there are no air molecules for the evaporated Aluminium to collide with, allowing it to travel further [5].

4.6 Lift Off

The lift off process is used to remove excess metal from the metallisation process from the device [5]. The sample is placed into acetone, a pipette is used to agitate the acetone. The acetone removes the remaining Photoresist and thus the unwanted Aluminium, any Aluminium bonded to the Gallium Arsenide sample will remain [5]. The devices are then cleaned using the process described in **Section 4.3** [5].

4.7 Ohmic Contact Fabrication

As described in **Section 3.2**, an Ohmic contact is formed by heavily doping the depletion region of the Metal Semiconductor junction. In practice this was completed by depositing a layer of heavily N doped Indium Germanium between the Gallium Arsenide and a Gold Contact [5]. The Indium Germanium acts as the depletion region for the junction, significantly increasing the chances of the electrons tunnelling through the barrier.

5 Device Characterisation

5.1 JV Characteristics

A probe station was connected to a Source Measurement Unit which could be controlled by Quick IV, a piece of software written by Keysight; this setup was used to automatically measure the current flowing through the Schottky Diode at varying bias voltages. An initial range of -3 to 3V, this was reduced to produce a curve without the reverse break down section of the IV characteristic.

Figure 3 shows the log(J)V Characteristics of the Schottky Diodes produced in the laboratory session. The devices have a varying diameter as shown in the graph legend. The devices show a logarithmic relationship between Voltage and Current Density; Current Densities are also similar between the differing device diameters.

From this graph approximate values of $J_0 = 0.018Am^{-2}$ and n = 2.91 can be calculated using **Equation 1** and **2** respectively.

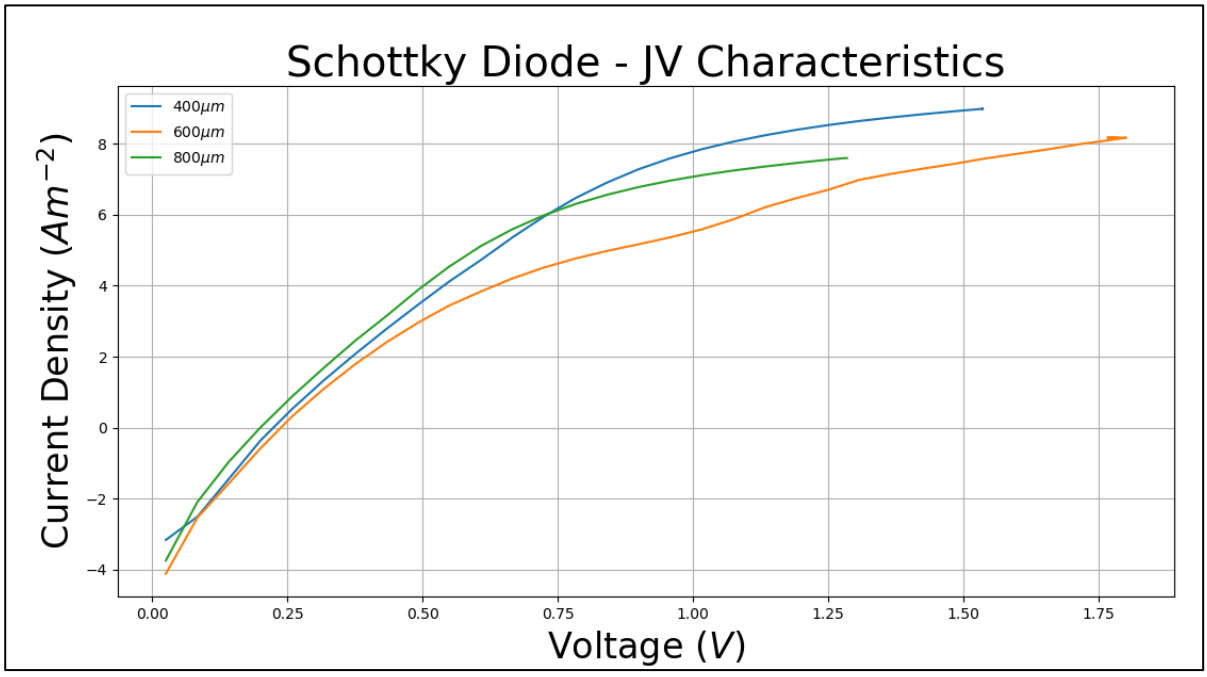

Figure 3: Schottky Diode JV Characteristics with varying device diameter

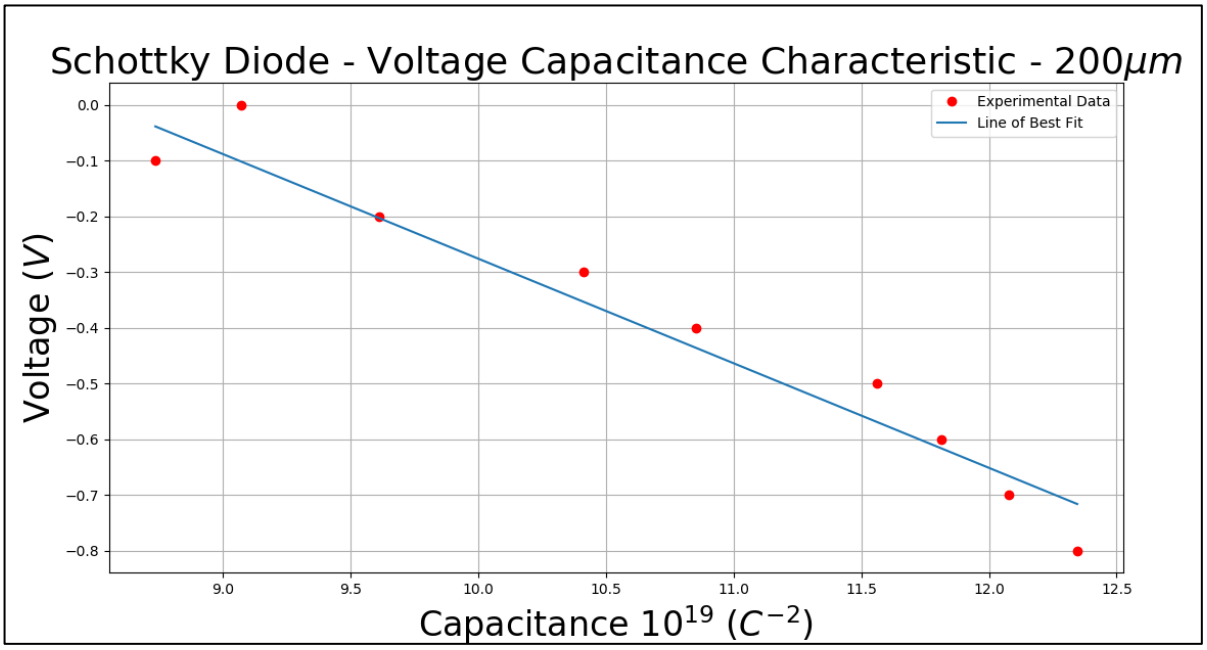

Figure 4: Voltage Capacitance Characteristic 200μm Schottky Diode

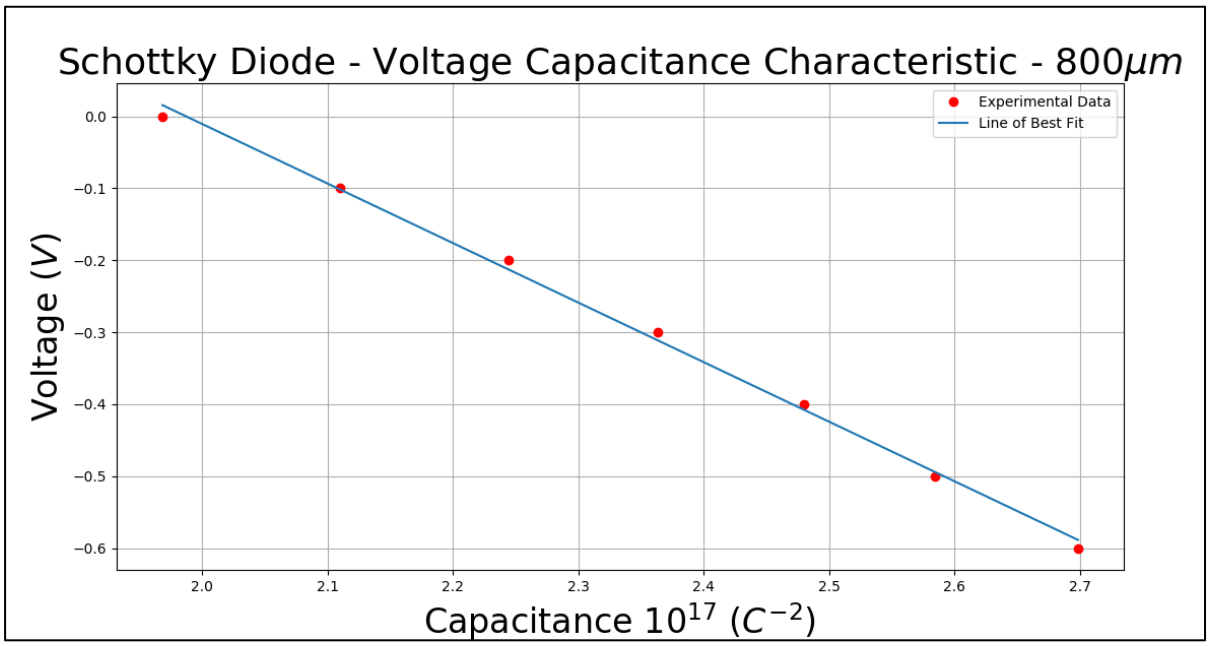

Figure 5: Voltage Capacitance Characteristic 800μm Schottky Diode

5.2 CV Characteristics

A probe station was connected to an LCR Meter, with one probe connected to the sample anode and the LCR meter grounded to the probe station base. The LCR Meter was used to measure the capacitance of the Schottky Diode at varying bias voltages. Due to the small capacitance of the Schottky Diode, the LCR Meter must be calibrated. Calibration is an automated measurement of the closed circuit and open circuit characteristics of the test equipment, which can then be used to calculate the test equipment capacitance. This calculated capacitance is then compensated for in the diode capacitance measurement. Negative bias voltages in steps of -100mV from 0V were applied to the diode.

Figure 4 and **Figure 5** show the measured Voltage Capacitance Characteristic of a 200µm and 800µm device diameter Schottky Diode respectively. Both devices show an inversely proportional relationship between V and C^{-2}. The capacitance decreases with decreasing device diameter. It is important to note that the data presented for the 200µm device diameter is sample data [6], due to issues with running the experiment when the laboratory was conducted.

From these graphs' approximate values of $V_{Barrier}$ = 1.4V and 1.58V and N_d = $1.87x10^{24}$ and $3.43x10^{24}$ can be calculated using **Equation 4** and **3** respectively.

6 Discussion and Conclusions

The JV characteristics from **Section 5.1** show behaviour like that shown in **Figure 1**. As expected from a rearrangement of **Equation 1** there is a logarithmic relationship between Current Density and Voltage in the Schottky Diode devices produced in the laboratory. Current densities are similar, as would be expected given that the diodes were made with semiconductor of the same nominal donor density. Deviations between the curves are likely explained by differing series resistances/capacitances and donor densities due to impurities introduced in the fabrication process from the air. The reverse saturation current densities shown are lower than that shown of commercially available Schottky Diodes, again however this is likely due to series resistance introduced in the fabrication process.

The CV characteristics shown in **Section 5.2** show the inversely proportional relationship between V and C^{-2} predicted by **Equation 3**. As expected from **Equation 4** the capacitance of the devices decreases with decreasing device diameter. The calculated values of N_d ($1.87x10^{24}$ and $3.43x10^{24}$ for 200µm and 800µm respectively) are similar, this would be expected as the semiconductor is provided pre-doped by the manufacturer where very accurate doping levels can be achieved. The high barrier voltages calculated (1.4V and 1.58V for 200µm and 800µm respectively) may be due to a series resistance provided by the ohmic or rectifying contact and by surface states in either of the junctions as described in **Section 3.2**.

In conclusion, the devices behave as described by the theory introduced in **Section 3**. The low capacitances exhibited make the diodes good candidates for high speed switching applications, however the high series resistance and barrier voltages indicate that too many impurities have been introduced in the fabrication process. This is likely due to the ISO class of the clean room used to fabricate the devices; clean rooms with higher air purity (and no human interaction) are used for the mass production of these devices in industry.

7 References

[1] G. Williams, “Semiconductor Laboratory: Fabrication and Assessment of a Schottky Diode - Background and Theory,” The University of Sheffield, Sheffield, 2018.

[2] J. Allison, “Metal-semiconductor junctions,” in *Electronic Engineering Semiconductors and Devices*, Maidenhead, Berkshire: McGraw Hill, 1990, pp. 178 - 184, 190 - 191.

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8 Appendices

8.1 800µm CV Data Table

Bias Voltage (V)	Capacitance (nF)	Phase Angle (°)
0	2.254	-87.05
-0.1	2.177	-87.31
-0.2	2.111	-86.14
-0.3	2.057	-84.08
-0.4	2.008	-81.06
-0.5	1.967	-77.33
-0.6	1.925	-72.79

8.2 200µm CV Data Table

Bias Voltage (V)	Capacitance (pF)
0	105
-0.1	107
-0.2	102
-0.3	98
-0.4	96
-0.5	93
-0.6	92
-0.7	91
-0.8	90